A585/A575/A565

Series of Advanced Mixed-Signal Test Systems

System Description

TERADYNE

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A585 Advanced Mixed-Signal Test System

A575 Advanced Mixed-Signal Test System

A565 Advanced Mixed-Signal Test System

Introduction

TESTING STRATEGY FOR MIXED-SIGNAL DEVICES

Device functionality continues to become more highly integrated, with analog functions on traditionally "digital" devices and digital functions and controls on formerly all analog devices. Whether you come from a formerly all analog or all digital testing world, the devices you must test now are mixed-signal devices. You may know them as "systems on a chip," "mixed-signal ASICs," or "system silicon". However you know them, these devices require a high-performance mixed-signal test system to successfully test both the components within each device as well as the overall system functionality of the device. The Teradyne A585/A575/A565 Series of Advanced Mixed-Signal Test Systems simplify the transition from all analog to analog-with-digital, or mixed-signal, testing because the addition of testing digital signals is handled in a manner familiar to you. Similarly, the transition from all digital to mixed-signal testing (with dynamic analog measurements) is also simplified because the architecture throughout the Teradyne A585/A575/A565 Series of Advanced Mixed-Signal Test Systems is based on the familiar per-pin functionality of VLSI test systems.

FUNCTIONAL VERSUS COMPONENT TESTING

To reduce time to market and ensure the greatest number of design-ins, device problems must be eliminated as early in the development cycle as possible. With the A585/A575/A565 series of test systems, semiconductor manufacturers can use one test program on a single test system to implement both component and functional test during the characterization phase of new silicon. This can significantly shorten the development cycle time.

During component testing, individual device building blocks are accessed and tested as discrete units. Performance is verified and faults are identified. In the development cycle, this information can be used to modify the design and eliminate the problem. On the production floor, this same component test will identify a failure that would impact overall device operation.

Functional testing ensures that the building blocks work together and the device functions as intended. Functional testing also helps to correlate faults at component test with functional performance errors. In addition, functional test guarantees that the system silicon meets the required industry standard specifications for Ethernet, ISDN, modems, video, and other mixed-signal devices, allowing a manufacturer to differentiate his product by guaranteeing performance with greater test coverage. Those manufacturers who verify the most specs on the device and price the device economically have a significant market advantage over other vendors of similar devices.

An example of functional and component testing can be demonstrated with the programmable filter device shown in figure 1. It contains an A/D converter that converts an analog signal to a digital signal for processing by the on-board DSP engine. The filter also contains a D/A converter for generating an analog output. A number of tests can be performed by accessing the components through the microprocessor bus: the converters can be isolated and tested for ac linearity performance, the DSP engine can be logically tested with high speed digital patterns, and the ROM contents can be read back to confirm that proper values have been programmed. Once the components are verified, an analog signal filtered by the device and captured by the test system can be analyzed for frequency response.

Running only functional tests would require 256 frequency response tests to ensure that all filter settings work correctly. However, system functionality can be verified with only one or two frequency response tests if the component tests are run first to verify the digital signal processor and that the coefficients are correct and readable from the ROM. This second strategy saves substantial test time in the production environment by combining functional and component testing.

The A585/A575/A565 series revolutionized component and functional test with the ability to run both types of tests on a common system platform with one test program. Numerous manufacturers around the world currently implement this strategy to test Ethernet, ISDN, video processors, disk drives, palette DACs, CODECs, multimedia, mixed-signal ASICs and other mixed-signal devices.

DEVICE TESTING SYNCHRONIZATION

Mixed-signal device testing requires that the digital pins and the analog instrumentation in the test system be synchronized. For example, if an analog source is programmed to generate a 1 MHz sine wave, and the digital pins are programmed to generate a 24 MHz pattern, each instrument must use the same timing reference to ensure that analog signal and digital patterns are locked together and repeatable. In order to accurately measure mixed-signal device performance, the analog waveforms and the digital data generated by the D/A and A/D

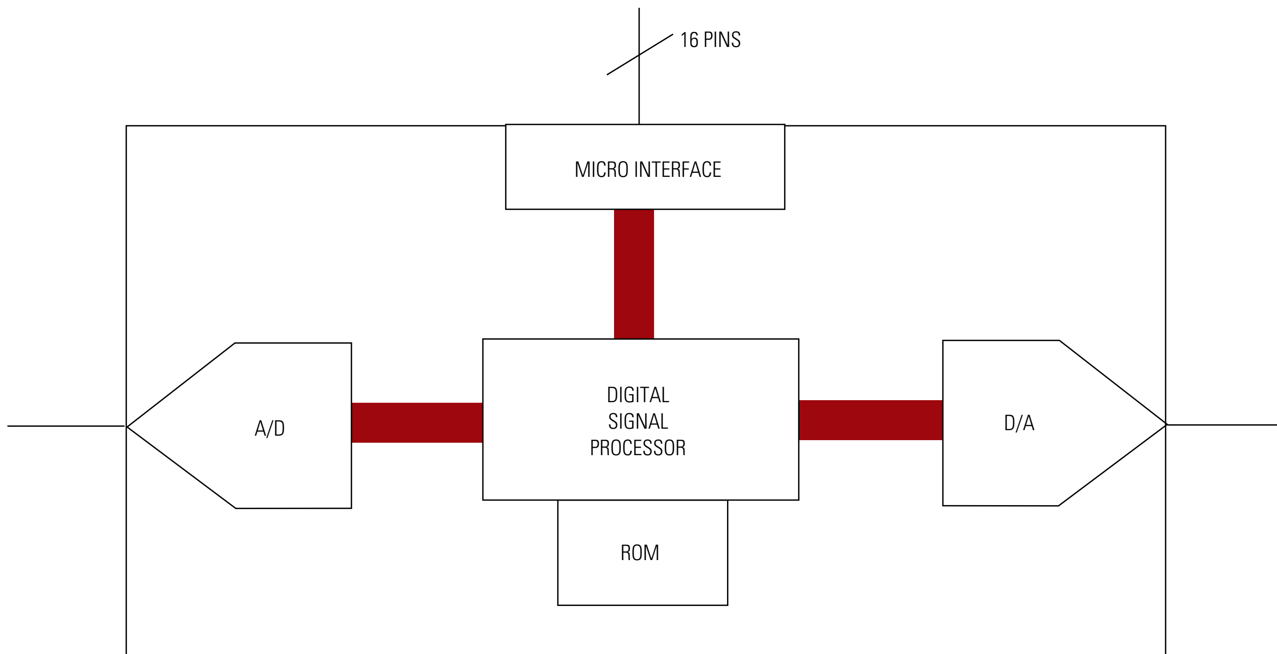


Figure 1
Block Diagram of a DSP programmable filter with 256 filter selections

converters on the device need to be synchronous with input signals in order to use digital signal processing to determine test results.

COMMON SYSTEM-LEVEL INTEGRATION

In each A585/A575/A565 series mixed-signal test system, Teradyne's innovative Vector Bus® III architecture is used to provide integration and synchronization of the digital pins and analog instruments. High performance instrumentation is common to the entire family of test systems. The Universal Bus architecture provides additional waveform distribution and timing synchronization between instruments. Finally, Teradyne's Interactive Menu-Assisted Graphics Environment, or IMAGE™, software environment is used for program creation, debugging and execution. Each of these elements is integral to the systems described in this System Description. See figure 2.

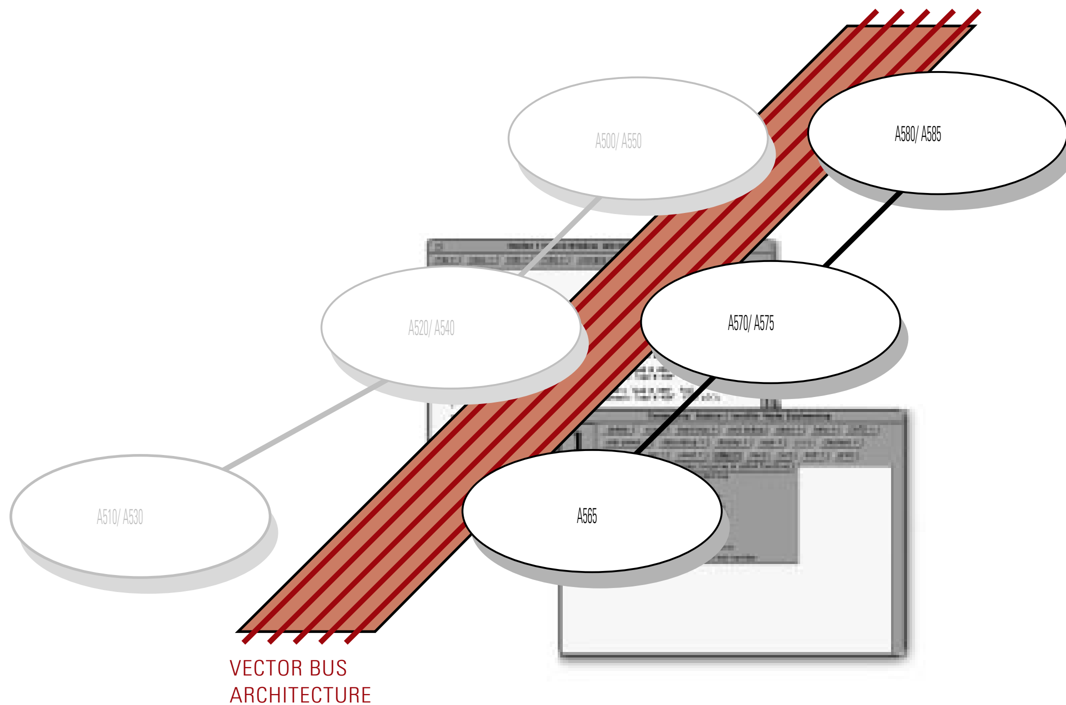


Figure 2
The Evolution of the A500 Family and the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems

The Evolution From VLSI To Mixed-Signal Testing

Because the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems share a common architecture with VLSI test systems, the transition from all digital testing to digital with dynamic analog measurements and mixed-signal testing is greatly simplified. As shown in figure 3, each block of the digital portion of the mixed-signal test system is the same as a VLSI test system. The digital per-pin channel architecture consists of:

- Digital Pattern Controller
- Digital Pattern Memory
- Digital Formatter and Timing Generator
- Digital Channel Card

The Digital Pattern Controller controls the execution of digital patterns and provides the ability to loop a pattern, to implement vector subroutines, to jump on fail, and to execute other functions that compress the pattern memory requirements of VLSI components.

The Digital Pattern Memory contains the pin state information required by the device under test (DUT). It sends the drive to 1 or 0, and the compare L, H, X or M states to the formatter and timing generator.

The Digital Formatter creates edges and waveshapes for the data such as return to zero or complement sur-

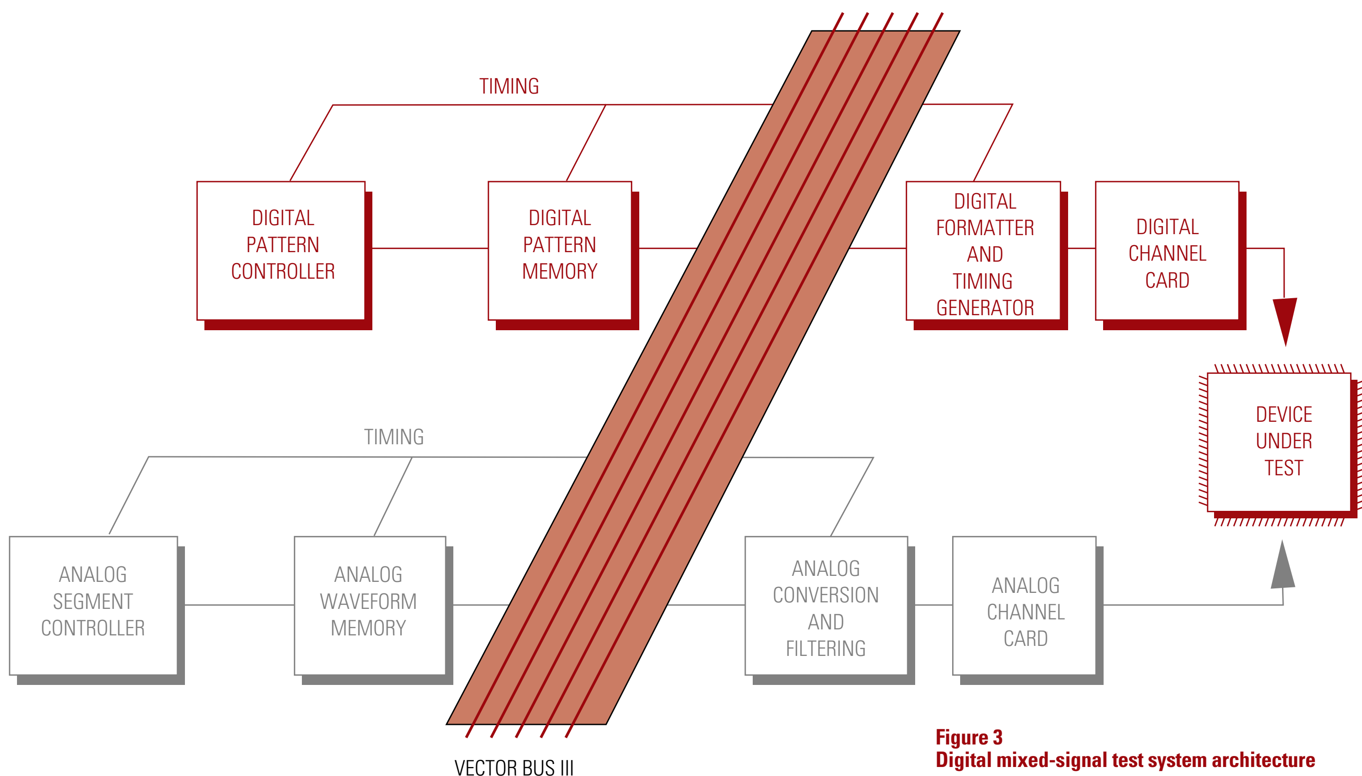


Figure 3
Digital mixed-signal test system architecture

round. The timing generator controls when the edges are applied. This information determines when the DUT receives data and when device generated data is strobed to evaluate its logic states.

The Digital Channel Card provides a controlled electrical interface for the digital signals to the DUT, with level control of the digital driver and voltage thresholds for the comparators on the channel card.

The analog signal sources and measurement capabilities of the mixed-signal test system are architected in a similar manner to that above. The building block concept of the VLSI architecture is applied to the analog instrumentation, as shown in figure 4, with four basic analog building blocks:

- Analog Segment Controller
- Analog Waveform Memory
- Analog Conversion and Filtering
- Analog Channel Card

The Analog Segment Controller is analogous to the Digital Pattern Memory. It governs the waveform memory sequencing, which contains digital samples representing the analog waveform that will be produced. Controller functions include looping, repeating, and executing the subroutines that generate complex waveforms for testing devices such as video processors and multimedia components.

The Analog Waveform Memory contains the digital samples that represent the analog waveforms to be produced. Segments of the waveform memory contain the digital representation of independent analog waveforms that, under control of the Analog Segment Controller, can be called in whatever sequence is needed to generate as complex an analog waveform as necessary to test a device.

The Analog Conversion and Filtering block converts the digital waveform samples to a continuous, full scale analog waveform, and filters it to

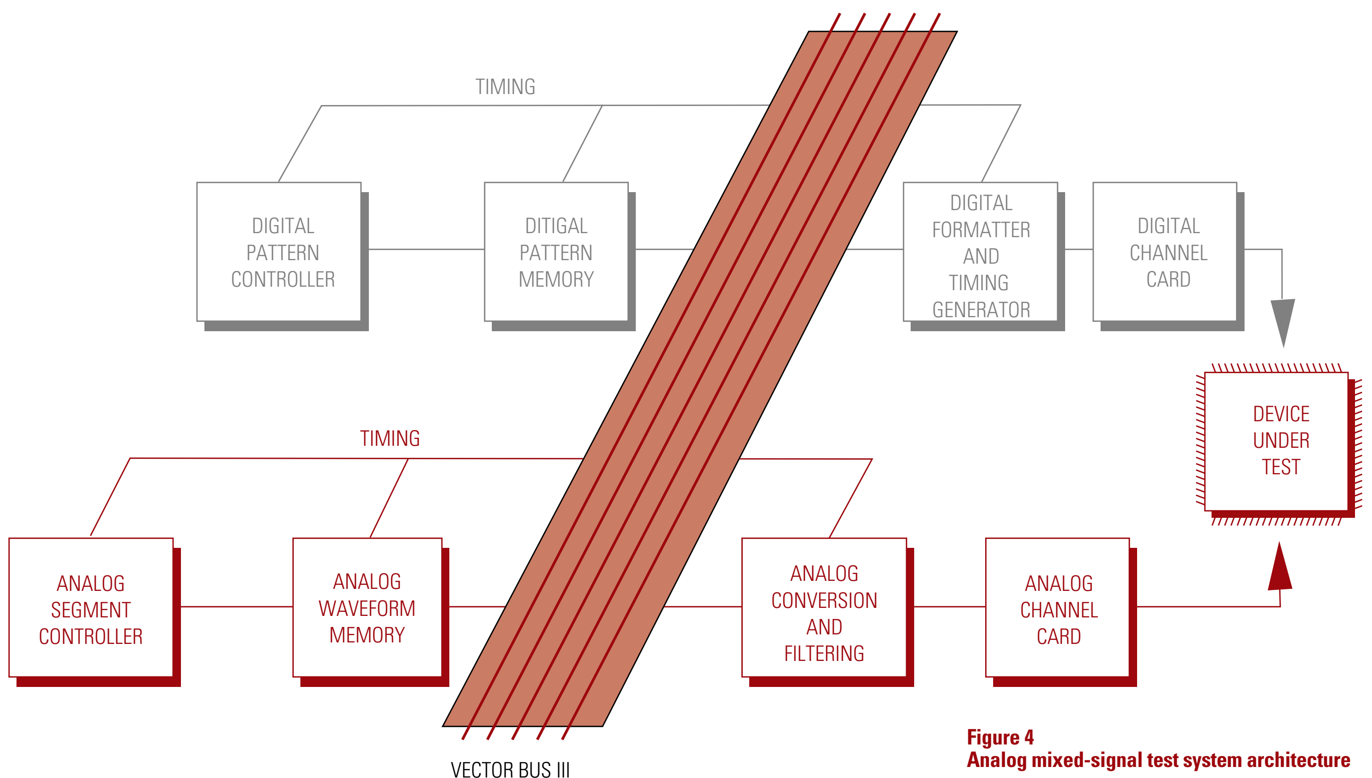


Figure 4
Analog mixed-signal test system architecture

remove any extraneous high frequency components that result from the conversion process.

The Analog Channel Card adjusts the amplitude, offset and impedance environment of the signal prior to its application to the DUT.

Because the analog and digital instrumentation are handled on a per pin basis and are configured with the same building-block architecture, programming the analog instruments is very similar to programming the digital instruments and these capabilities can support both component and functional testing. Test programs can be developed and placed on-line quickly.

An example of just one area where an A585/A575/A565 series mixed-signal test system can reduce test time development over a VLSI test system, is when measuring time between events in testing digital functions, pseudo-asynchronous events or phase locked loops, etc. In the VLSI test system, an edge find using a binary search is used to determine when a digital edge occurs, and is repeated to determine time between two events.

The edge find algorithm can consume both a great deal of development time to implement and more test time than desired in production. In the A585/A575/A565 mixed-signal test systems, the time between events can be measured directly with an analog instrument used for time measurement in a “single shot,” making it easy to program and fast to execute.

The Evolution From Analog To Mixed-Signal Testing

The A565 member of the A585/A575/A565 series of test systems can be configured as an analog only system. However, as your test requirements grow, digital instrumentation can be added. Thus the analog test techniques that you are accustomed to can be used in analog testing as well as with analog devices containing digital or integrated mixed-signal devices. In the same manner that the instruments in an analog test system share a common timing reference in order to be synchronized, the digital instrumentation in a mixed-signal system is also tied to the same reference. This ensures that both analog and digital signals will be synchronized so that Digital Signal Processing techniques can be used to make the test measurements. See figure 5.

When performing analog testing, the DUT output can be sampled by an analog digitizer and stored in a capture memory to be processed later. If the device output is digital data from an A/D converter, the mixed-signal test system can capture the waveform samples into a memory to be processed later.

When generating waveforms into the device, the analog test system provides a memory-based instrument where samples of the waveform are stored. The waveforms are described in terms of level, frequency, phase and waveform type. If the device requires digital inputs to a D/A, then the mixed-signal test system has a memory in the digital instrumentation that is just like the analog instrument where samples of the waveform are stored. The waveform samples are described just like an analog instrument in terms of level, frequency, phase and waveform type.

With the waveform sourcing and measuring in common between the analog and digital portions of the test system, programming the A585/A575/A565 series of mixed-signal test systems is straightforward.

Another commonality between the analog system and a mixed-signal system is in measuring dc characteristics of the device pins. Just as an analog system provides a V/I per pin capability, the mixed-signal test system can do the same with the addition of a V/I per digital pin. This capability provides for the easy development and fast execution of continuity and leakage testing on all device pins.

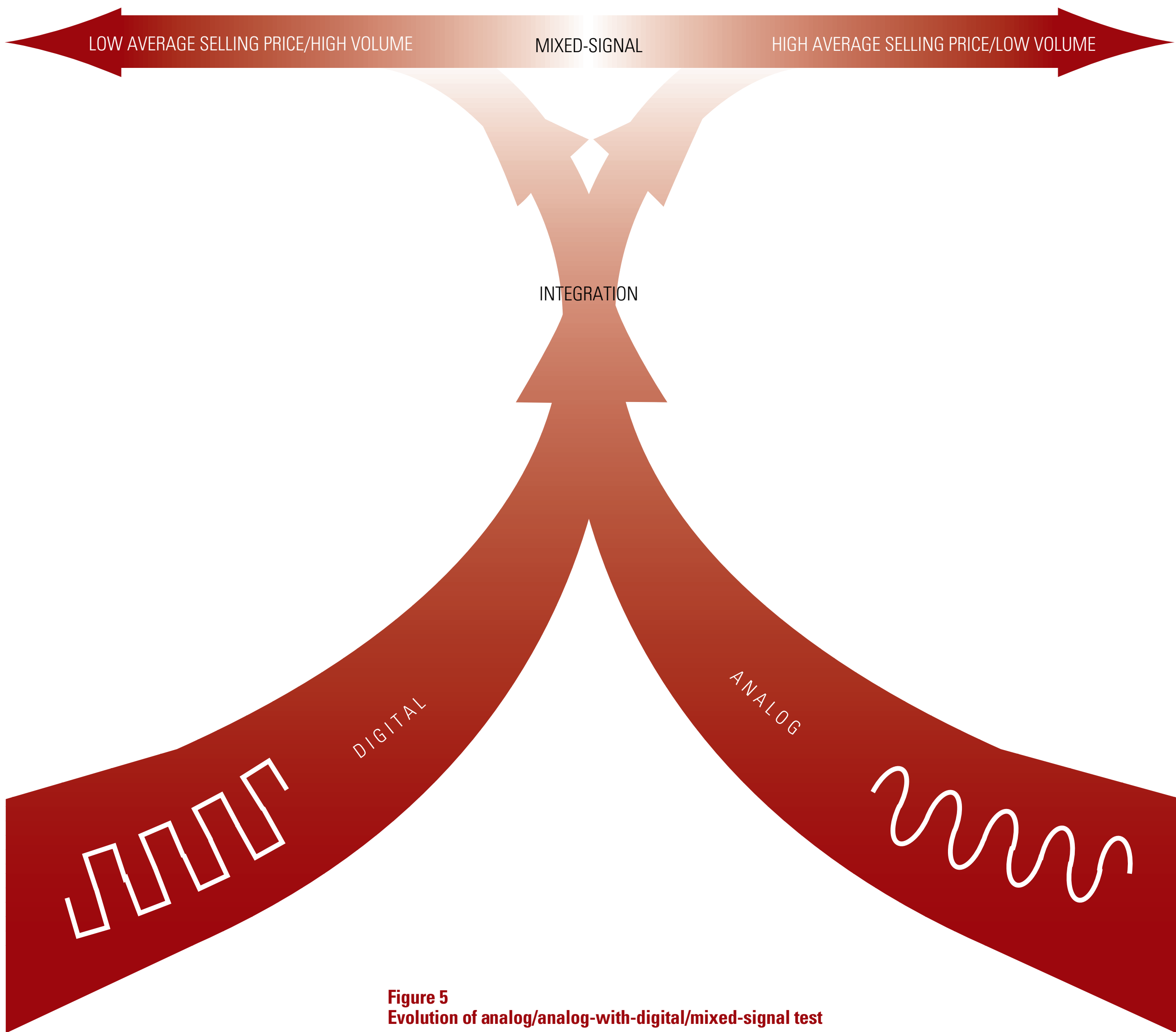


Figure 5
Evolution of analog/analog-with-digital/mixed-signal test

The A585/A575/A565 Advanced Mixed-Signal Test Systems

Regardless of your testing experience, mixed-signal testing in the A585/A575/A565 series mixed-signal test system environment will be familiar to you. The building-block architecture, synchronization between analog and digital instruments, and the IMAGE programming environment, all contribute to the high level of integration within the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems.

Each of the test system models within the A585/A575/A565 series are subsets of one another. Most of the analog and digital instruments are available for any of the models in the series. The maximum number of pins supported and the maximum number of instruments contained within each system reflects the limitations of each. For additional information regarding the specific system configurations, please refer to the System Configuration section of this document.

The A585 Advanced Mixed-Signal Test System provides the greatest configuration flexibility. A single system can contain up to 192 digital pins, support microwave instruments capable of generating 4 GHz and measuring 6 GHz analog waveforms, provide up to 750 volts dc with synchronized power instrumentation, and measure sub-picoAmps with advanced linear instrumentation. The digital pins support 200 Mbit/s data rates and both synchronous and asynchronous dual time domain testing. Options are available that support 400 MHz performance.

Despite its smaller footprint, the A575 test system can support up to 128 digital pins. Although the smaller cabinet limits the total number of instruments per single system, the A575 can be configured with much of the same analog and digital instrumentation available for the A585, with the exception of some synchronized power instrumentation.

The A565 is a highly modular test system. The basic A565 system supports instrumentation for any dc application. Power, ac or digital instruments can be added to create a low-cost mixed-signal test system, with performance similar to the A575 and A585 systems.

The following sections describe each system. Common elements include:

- Vector Bus III Architecture
- Universal Bus Architecture
- Dual Computer Architecture
- IMAGE Software System

The Vector Bus Architecture

The Vector Bus III illustrated in figure 6 is the foundation of the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems. Five key features provide the flexibility needed to test current and future mixed-signal devices:

- TimeMaster™ Clock Synchronization
- MultiSource Data Mixing
- Mixed-Signal Microcode™ Control
- MultiSync TimeGen™
- MultiState Memory Store

TIMEMASTER CLOCK SYNCHRONIZATION

One of the most critical mixed-signal tester requirements is that both analog and digital instruments be synchronized to a common timing reference. The TimeMaster Clock in figure 7 provides the common reference for all analog and digital pins. The highly accurate 10 MHz reference, along with the frequency synthesizer and associated circuitry, generates an extremely low jitter clock that is programmable over a 160 MHz to 200 MHz range.

The digital and analog clocks are derived from the TimeMaster Clock. The digital subsystem generates two clocks: a C0 clock, also referred to as a device system clock, and a T0 clock, referred to as the data clock or the vector rate clock. The T0 clock drives the digital pattern cycle time.

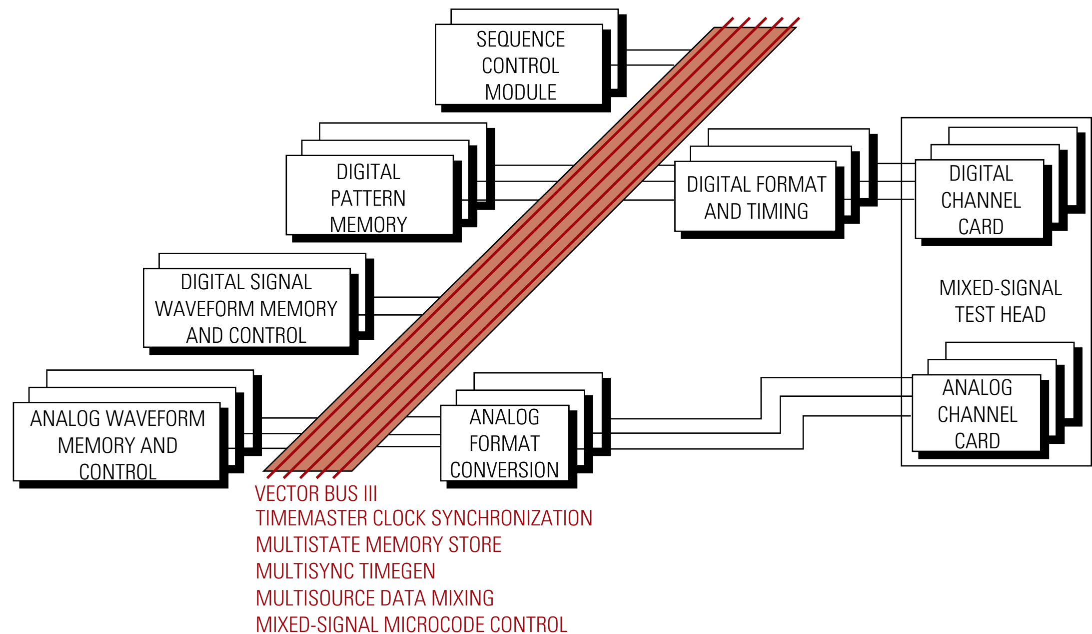


Figure 6
The A585/A575/A565 series Vector Bus III architecture

The C0 clock is an integer divide from the TimeMaster Clock and the T0 clock is an integer divide from the C0 clock. Clock rates range from 50 MHz or 25 MHz depending on the system configuration, down to 4.88 kHz. For example, when testing a microprocessor, the C0 clock may operate at 32 MHz and the T0 clock at 8 MHz. In this case, the digital patterns can be compressed in size and complexity by 4:1, eliminating the need to repeat data vectors.

The A585/A575/A565 series also provides 1,023 timing sets for per-pin timing changes on-the-fly while digital patterns are executing. The C0 and T0 clocks can be independently modified on-the-fly, permitting device read and write timing cycle changes that may be necessary when testing on-board memory.

The analog clocks in the test system include four integer clock dividers that provide independent generation of clocks from 2.5 kHz to 50 MHz. These clocks distribute timing to all ac instruments. Each ac instrument can select any analog clock as its sampling reference.

The A0 clock includes a feature required when generating analog signals that contain program controlled jitter. Microcode commands that increment and decrement the A0 divide value can be issued from the digital pattern. These commands, which can be issued to the A0 clock at digital vector rate speeds of 50 MHz or 25 MHz depending on system configuration, allow generation of triangular, sinusoidal, and multifrequency jitter patterns.

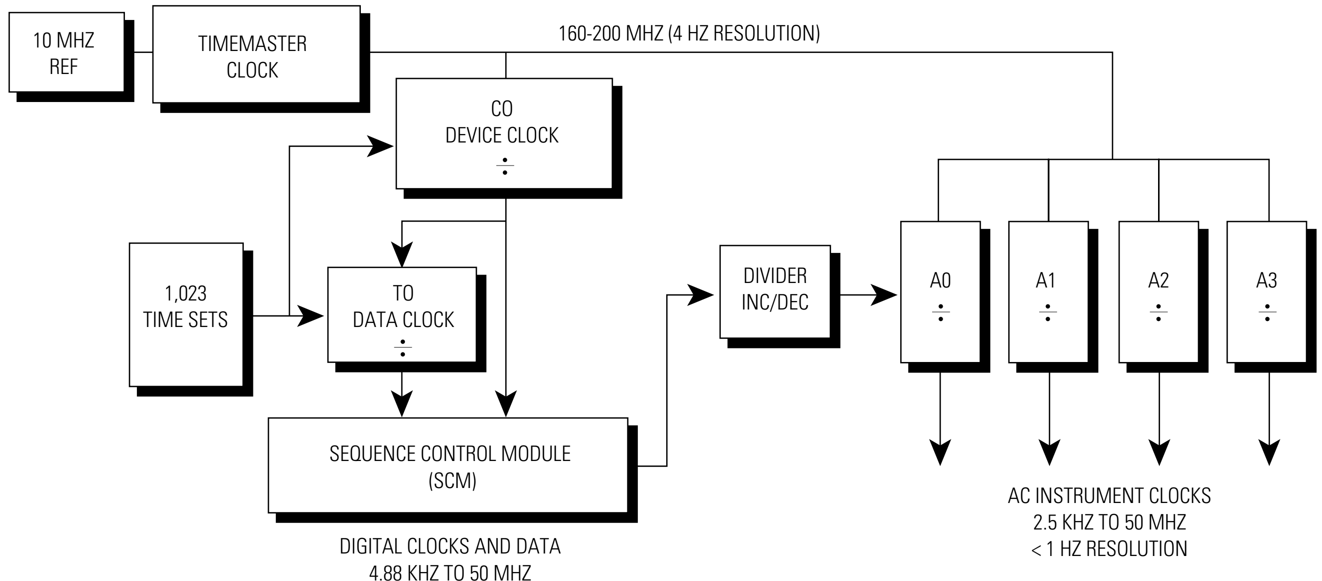


Figure 7
TimeMaster Clock Synchronization

MULTISOURCE DATA MIXING

Mixed-signal and VLSI device testing require that digital patterns exercise the digital blocks. When performing truth table tests, a digital pattern from digital design simulators can be used to drive and compare deterministic digital patterns.

In order to test devices containing D/A and A/D converter components, the test system must be able to generate or capture digital representations of analog signals also referred to as digital signals. This data can be expressed as a sine wave at a specific frequency and level with a specific digital code format such as sign plus magnitude.

Since the data associated with testing an A/D converter is non-deterministic, the system must be able to capture the data rather than run a truth table comparison of the data. The captured data is then processed by the Digital Signal Processing (DSP) algorithms to determine performance of the A/D component.

Because many manufacturers are integrating SCAN technology for increased digital fault coverage, mixed-signal systems must have SCAN testing capabilities, which require very deep serial patterns of configurable pin width.

The Vector Bus III MultiSource Data Mixing provides additional memories in the A585/A575 for efficiently handling SCAN requirements and digital signal source and capture. The memories are available to any digital pin under program control. The Alternate Data Bus allows each digital tester pin to select digital pattern, digital signal, or digital SCAN capability, and provides the ability to switch the selections on-the-fly. See figure 8. Access to different types of memory with the Alternate Data Bus simplifies device interface board design by eliminating the need for "special" digital pins.

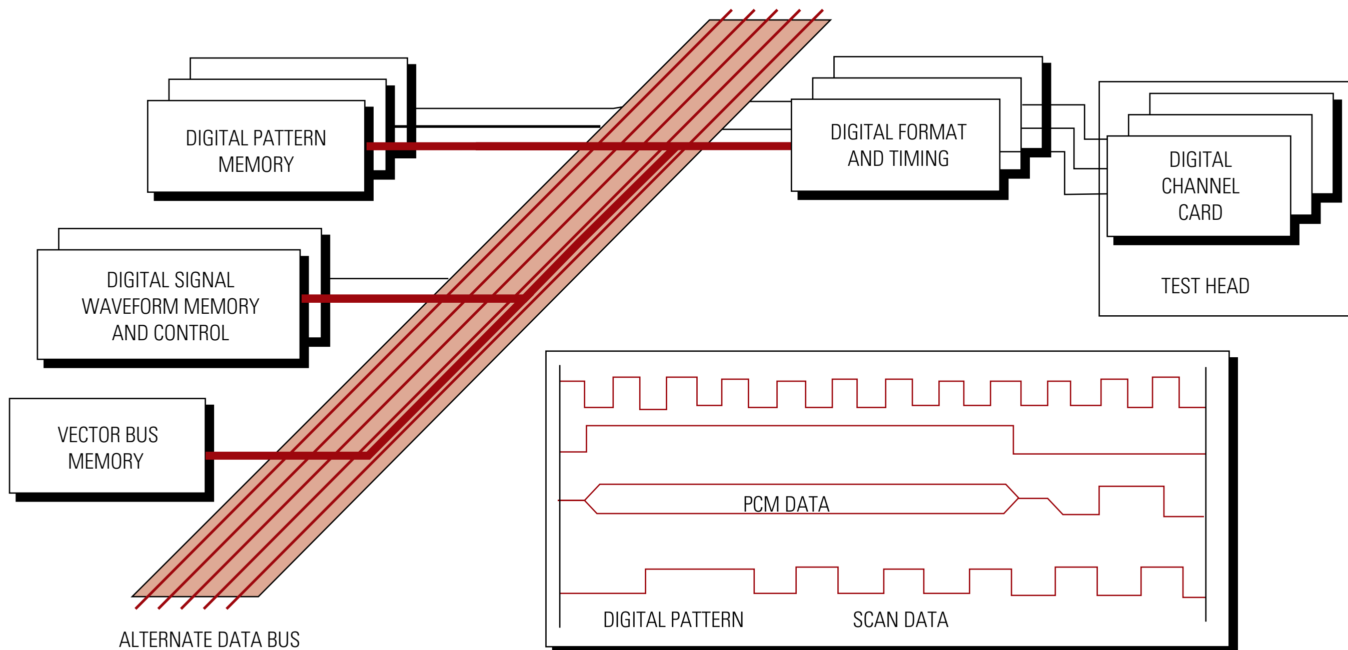


Figure 8
Mixing of SCAN, pattern and digital signal data selected per pin

MIXED-SIGNAL MICROCODE CONTROL

When testing AVLSI system silicon, the ability to control when analog instruments begin to generate waveforms or capture signals is critical. Mixed-Signal Microcode Control allows the digital pattern to deliver microcode commands to the analog instruments on a vector by vector basis, as illustrated in figure 9. This capability is referred to as Vector-Locking™.

Vector-Locking ensures repeatability. For example, as shown in figure 10, when testing an analog-in to analog-out function, an analog source could begin after 100 clock cycles. Then, after a 20 clock cycle settling time, the analog output could be captured with a waveform digitizer. Every time the program runs, the same waveform will be sent on the 100th device clock cycle, and capture will begin on the 120th clock cycle. This locking provides precise control of analog and

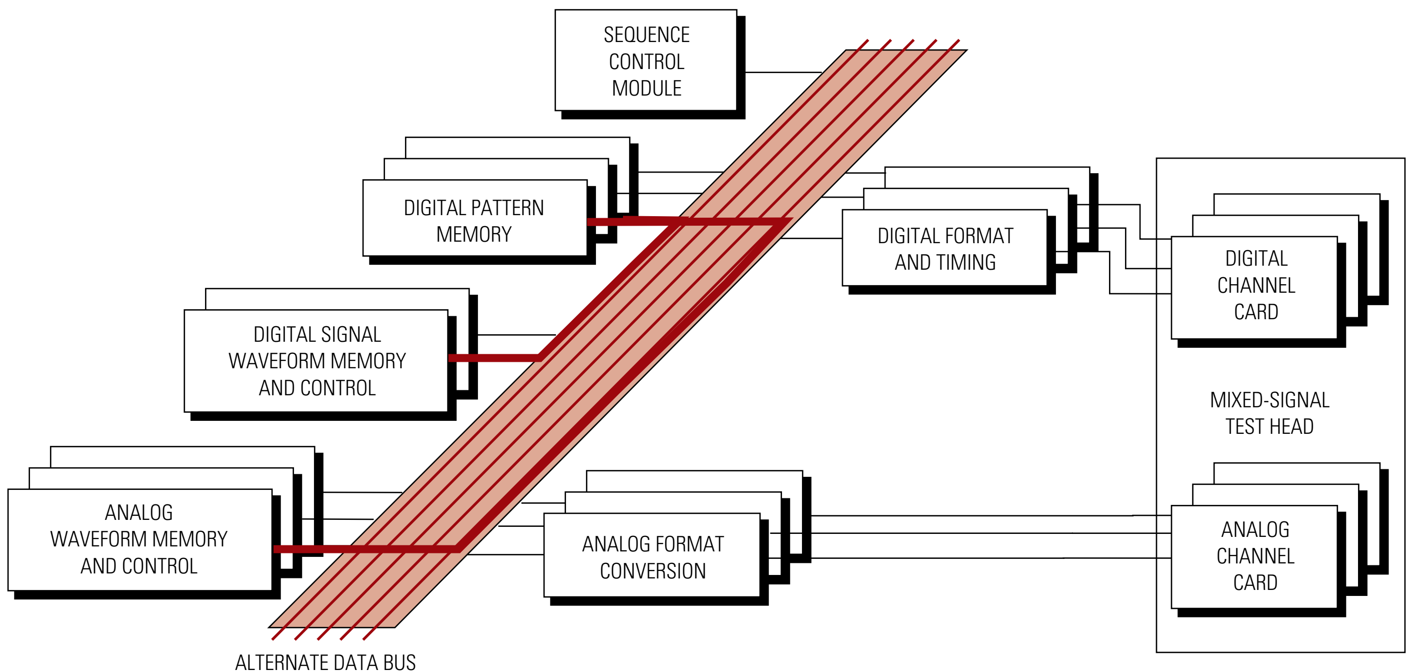


Figure 9
Vector Bus III delivers the Mixed-Signal Microcodes directly to the analog instrument memory controller.

digital waveforms and also enhances test measurement repeatability, reducing guardbands.

Vector-Locking is also used when testing a device that demodulates analog waveforms into digital bits, as in a FAX modem device. The digital pattern performing the bit comparison detects exactly when the analog signal began. If the analog source began under computer control, the starting phase would be different from the device clock phase. This phase discrepancy will cause errors in the bit stream that is generated by the device.

As shown in figure 11, each analog instrument has a unique set of microcode that is available at every digital vector.

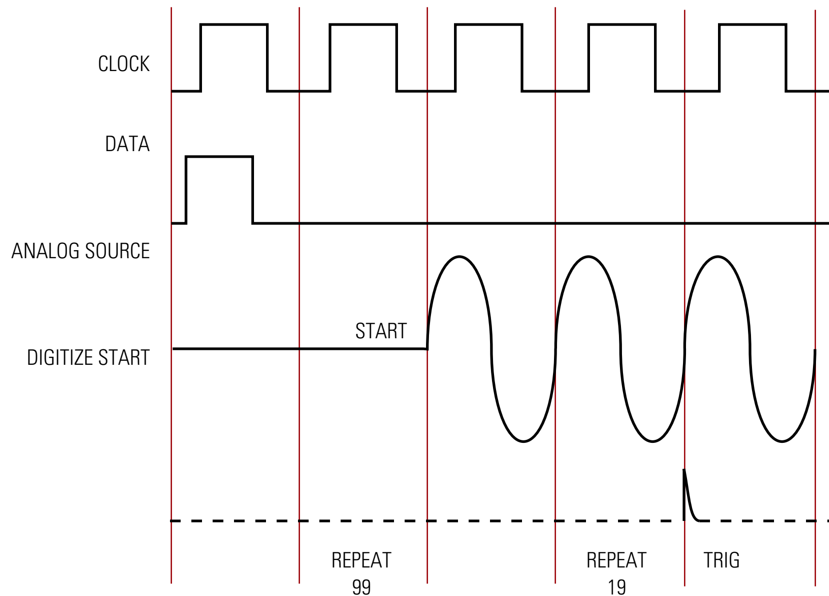


Figure 10
Mixed-signal microcode provides Vector-Locking between the analog and digital instrumentation.

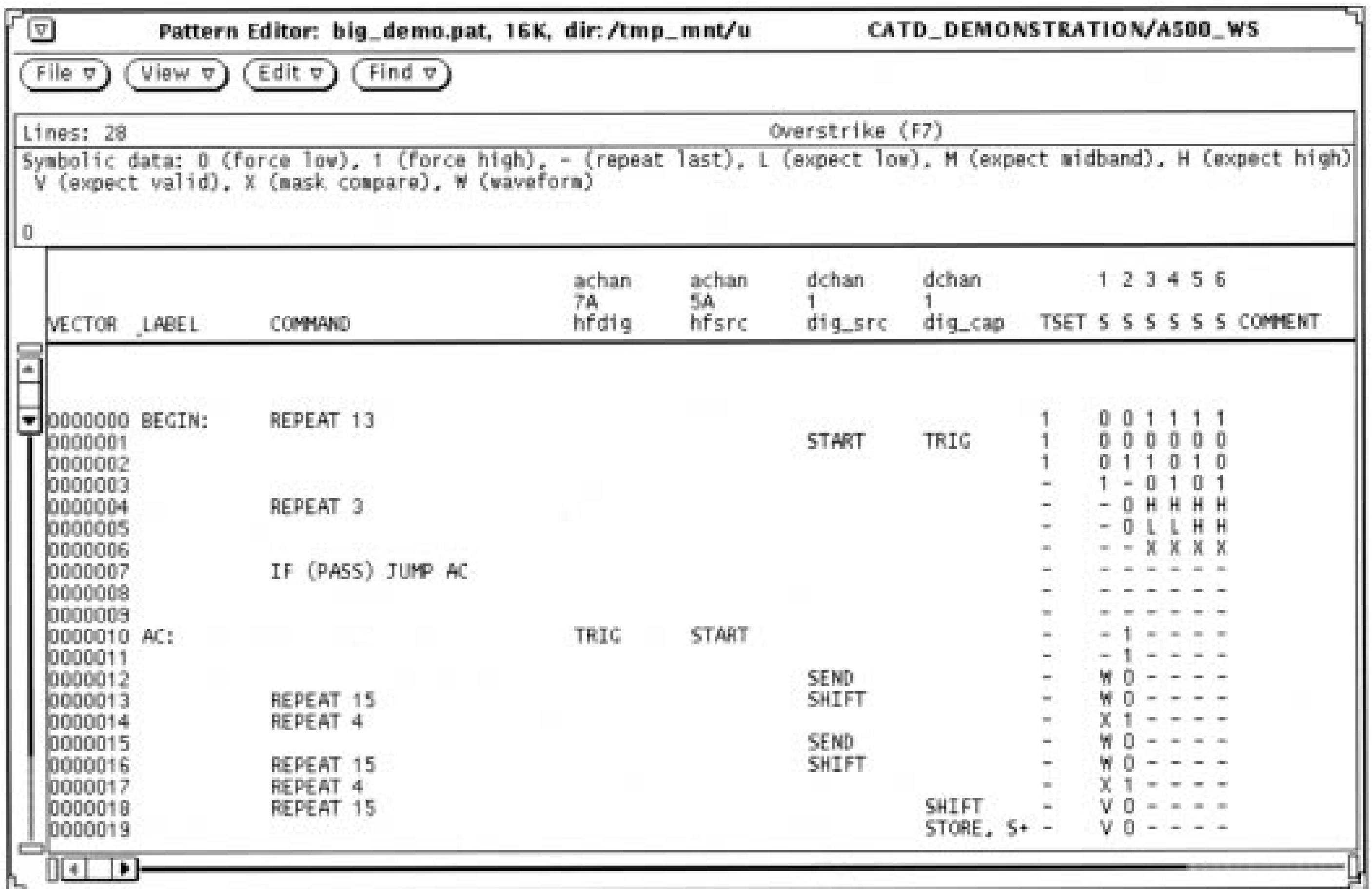


Figure 11
The Mixed-Signal Microcode is programmed in the digital pattern to control the analog instruments at each vector cycle.

MULTISYNC TIMEGEN

As mixed-signal devices appear in increasingly diverse applications, they must function in asynchronous environments. In particular, communications network devices must convert data over a wide range of frequencies to standardized frequencies for telephones and data terminals. The tester must simulate real world asynchronous problems so that the manufacturer can identify and correct device faults.

As shown in figure 12, the A585/A575 test system Vector Bus III architecture can be configured as a dual Vector Bus system. Essentially, two Vector Buses, two digital systems, and two sets of analog instruments can be assigned to different parts of the device, providing true asynchronous test capability. The two Vector Buses can handshake with each other to resynchronize and help perform fault diagnosis. This means the test system can perform as two separate mixed-signal test systems running asynchronously or synchronously.

MultiSync TimeGen can economically accommodate a multitude of applications. Some applications require only asynchronous analog signals while others require both asynchronous analog and digital signals. MultiSync TimeGen can be configured to meet any of these needs cost effectively, adding clocks or a dual digital sequencer as needed.

As shown in figure 13, MultiSync TimeGen may contain two master clocks: a TimeMaster Clock and an Alternate TimeMaster Clock. Digital and analog clocks can be programmed to either TimeMaster clock, providing maximum frequency flexibility. In addition, two auxiliary analog clocks, pro-

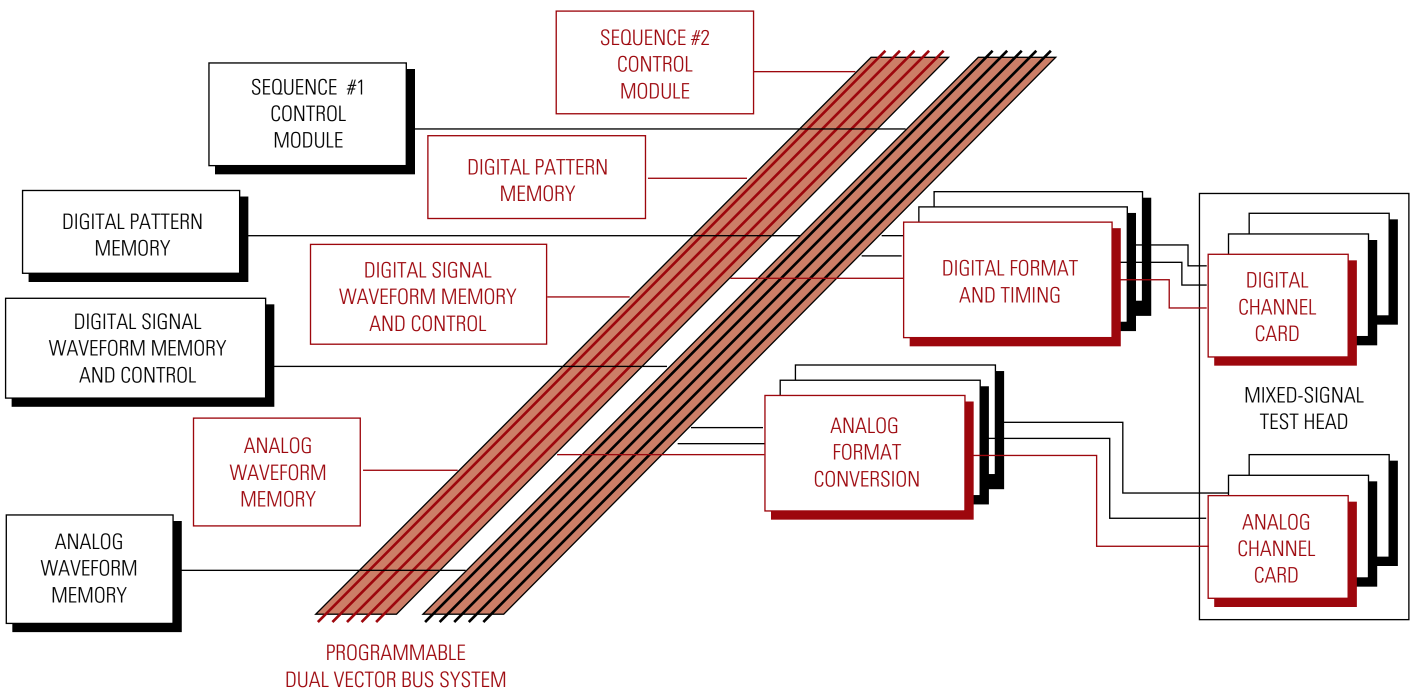


Figure 12
The A585 can perform synchronous and asynchronous testing using a dual Vector Bus system.

grammable from 40-200 MHz, are available for use with the ac instrumentation. There is also an Auxiliary TimeMaster Clock for use with the Sampler only. In order to guarantee frequency coherency, all clocks link to a common 10 MHz frequency reference.

MultiSync TimeGen also has an additional digital pattern sequencer. Groups of 64 digital pins can be programmed to select one of two sequencers. Each sequencer operates asynchronously. The second sequencer can use either the standard TimeMaster Clock or the Alternate TimeMaster Clock.

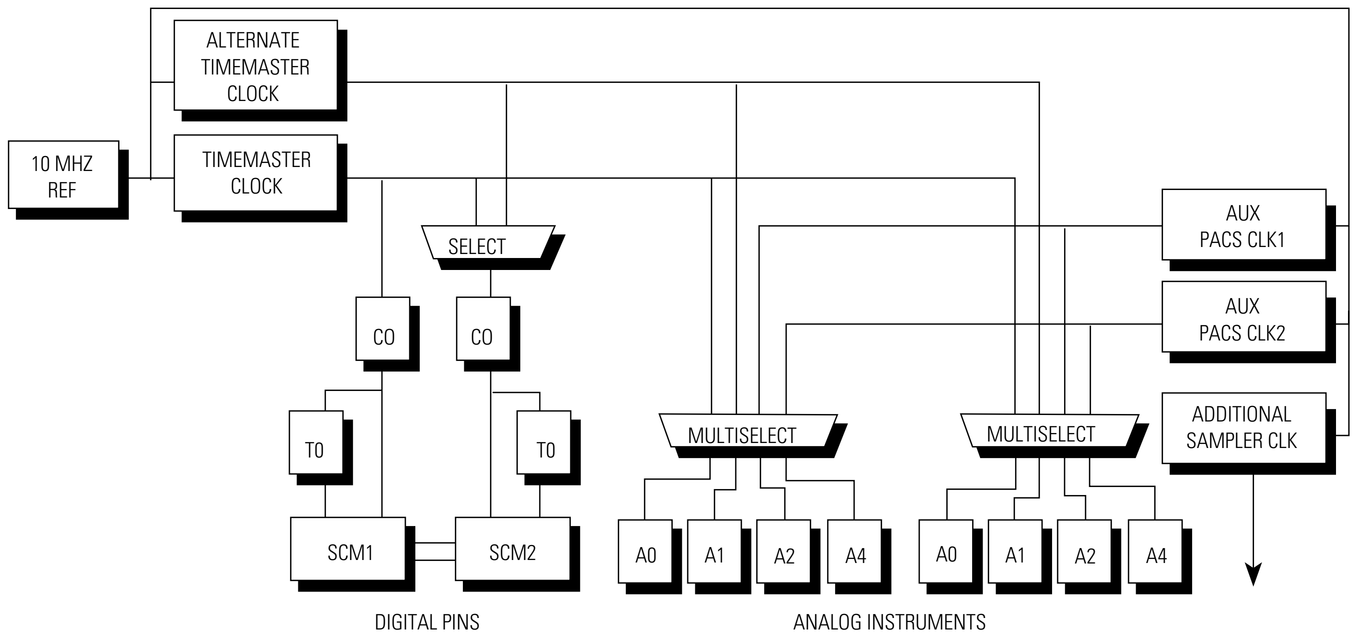


Figure 13
MultiSync TimeGen provides multiple clocks and two independent time domain systems for asynchronous testing.

MULTISTATE MEMORY STORE

The number of digital device pins and the combinations of operating conditions on analog pins are increasing rapidly, and all must be tested. A common AVLSI device test, four corner testing, requires a functional test at minimum/maximum timing conditions over minimum/maximum voltage. MultiState Memory Store, shown in figure 14, meets this requirement by providing a 1 Meg deep SETS memory that can perform high-speed reload of the digital channel card dc attributes (V_{IH}, V_{IL}, V_{OL} and V_{OH}) and high speed timing set reloads. Also, the Vector Bus memory can provide reload capability of pattern memory.

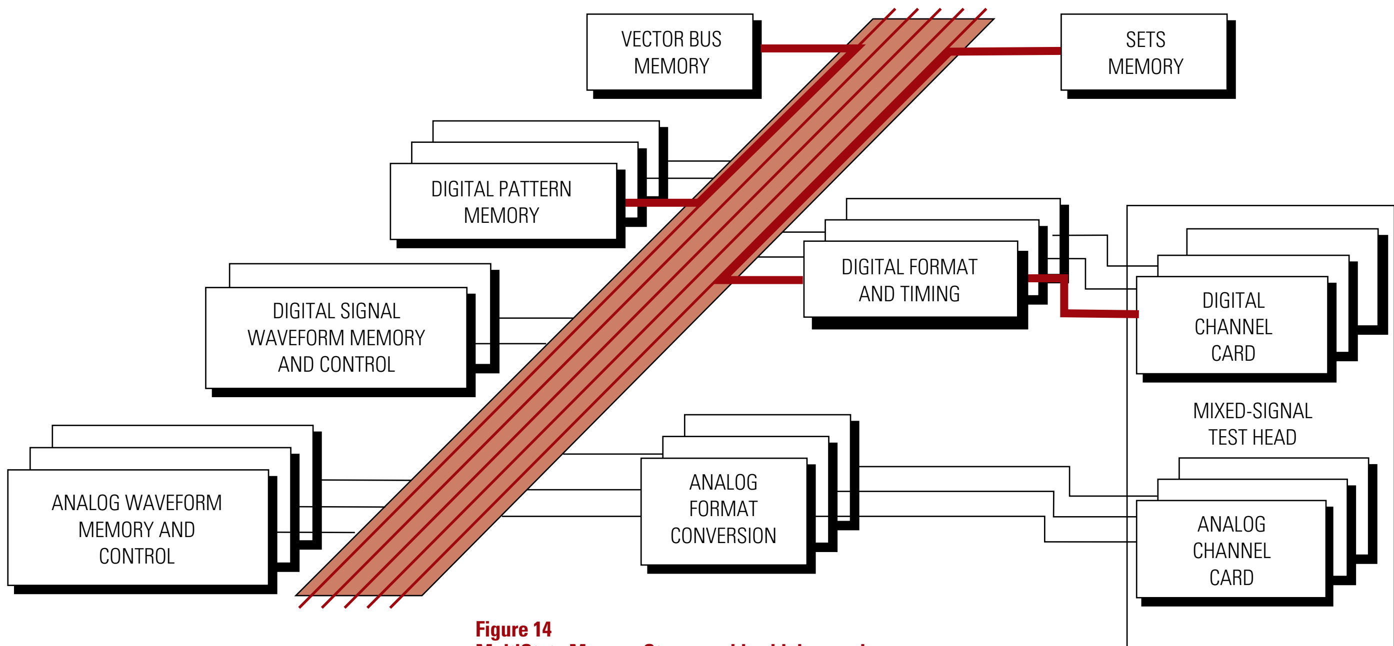


Figure 14
MultiState Memory Store provides high-speed reload of timing and dc attributes of digital pins and patterns for high pin count devices.

Universal Bus Architecture

Advanced analog and high power device testing requires synchronization and waveform linkages between instrumentation. Teradyne's Universal Bus architecture meets this need. See figure 15. Timing control of the DUT and tester instrumentation is critical when testing high power devices. While the high speed digital pins in the test system drive low power DUT control pins, the trigger driven power instruments deliver synchronized power events to DUT power outputs. When operating in pulse mode, the power instruments attain a high instantaneous power level. Control is critical. Proper timing prevents device destruction when evaluating parameters such as thermal die attach. Timing control ensures that measurements are not influenced by device warming due to power dissipation.

For example, consider testing the ON resistance of a FET switch that is embedded in a mixed-signal device. If a high current is sent through the device for too long, the FET ON voltage will begin to rise due to thermal runaway. Measurements must be made before this occurs. The power instrumentation timing control turns on the pulse for a predetermined amount of time, strobes the meter, and pulses the current on only long enough to make the measurement. See figure 16. A test engineer can also "trap" on this test without damaging the DIB circuitry.

The versatile Universal Bus architecture provides the control for high

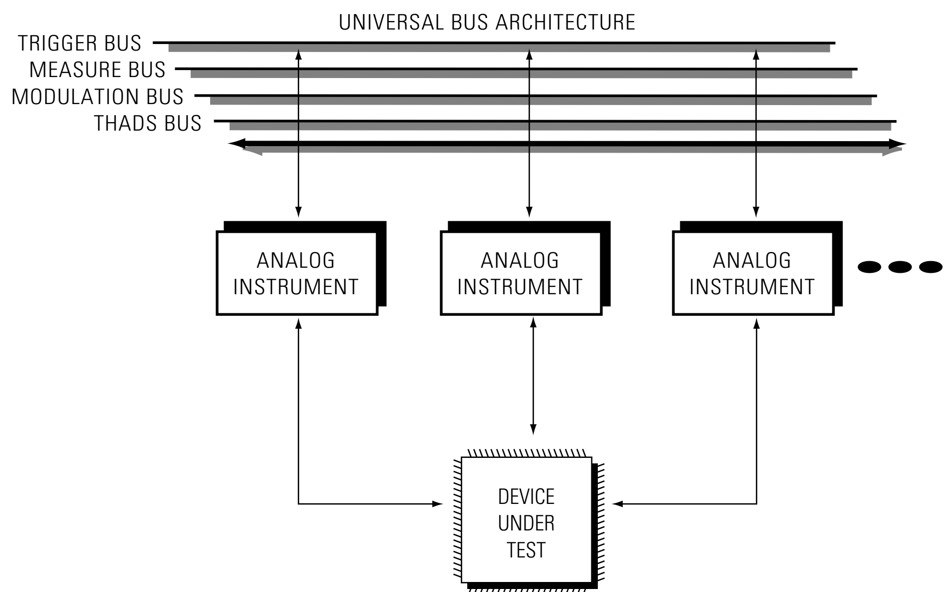


Figure 15
The Universal Bus Architecture

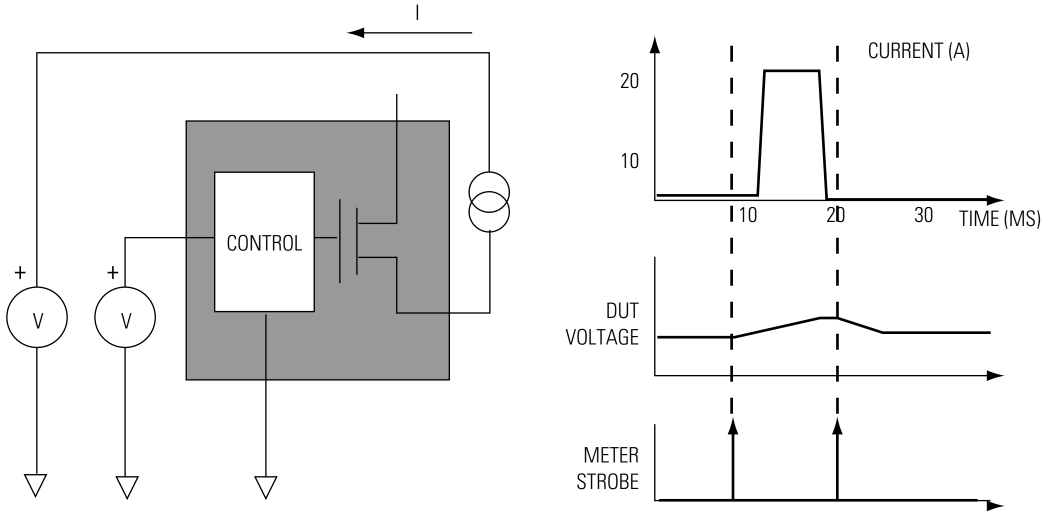


Figure 16
When the device dissipates substantial power, thermal effects can alter its measurements.

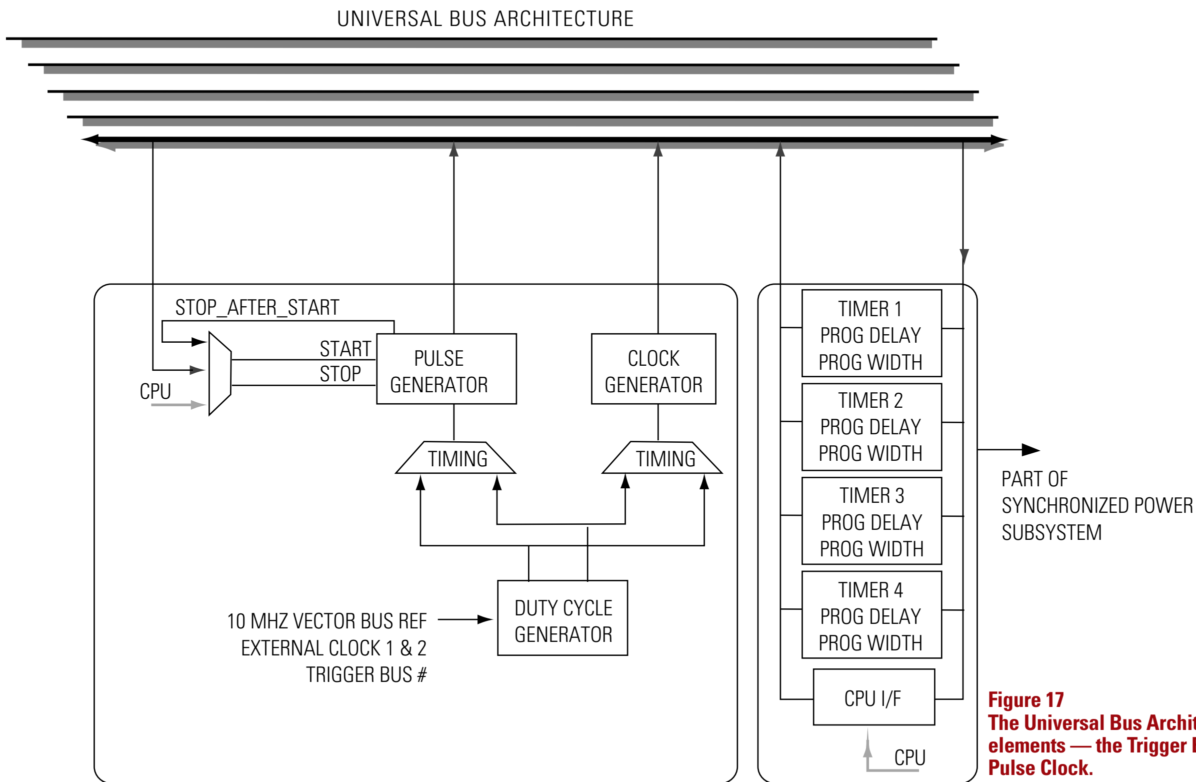


Figure 17
The Universal Bus Architecture has two timing elements — the Trigger Bus and the TimeMaster Pulse Clock.

quality, maximum throughput testing of analog and power components embedded in mixed-signal devices. It consists of four essential elements:

- Trigger Bus
- Measure Bus
- Modulation Bus
- Test Head Analog Distribution Bus (THADS)

TRIGGER BUS

The Trigger Bus is made up of a TimeMaster Pulse Clock and an internal timing bus. TheTimeMaster Pulse Clock provides multiple timing controls to the instruments in the test system. As shown in figure 17, there are two parts to this clock: a set of pulse generators for controlling power instruments and a repetitive pulse and clock generator for controlling advanced analog instrumentation. The pulse generators contain four programmable delay and pulse width timers with timing ranges from 1.3 ms to 1.6 s. Each timer has 200 ns programmable resolution. The timers can receive a start signal from the timing control bus or from the CPU.

The repetitive pulse and clock generator can receive reference input from a variety of sources. It can access the internal tester 10 MHz reference from the Vector Bus III, use one of two externally generated clock sources, or get a reference from another instrument connected to the Trigger Bus. Programmable dividers adjust the pulse width and frequency of the generated pulses. From the 10 MHz reference, the TimeMaster Clock can generate pulse widths from 100 ns to 6553.6 µs and frequencies from 10 MHz to 153 Hz. The clock can be sourced to a timing control bus as a clock signal, or can be gated on and off directly from the test program or from other bus signals. A pulse counter can stop the clock after a predetermined number of pulses.

The Trigger Bus also contains an internal timing control bus that connects all synchronization signals between the instruments and the TimeMaster Pulse Clock through eight differential ECL lines. See figure 18. Every instrument that interfaces to the Trigger Bus can receive or send synchronization signals through one of the eight trigger lines.

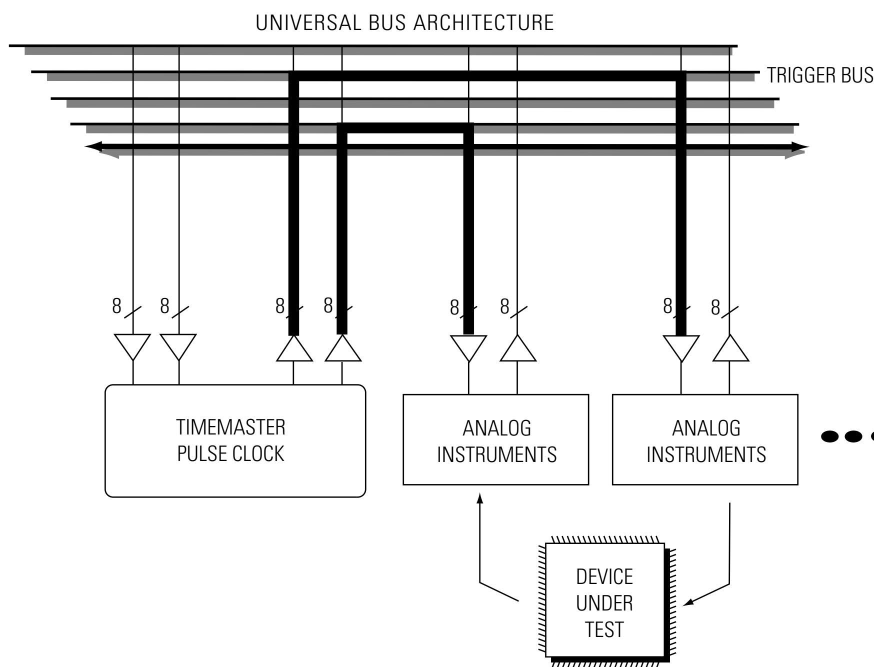


Figure 18
The Trigger Bus provides well-controlled, repeatable power testing by connecting the timing of all the power and analog instruments together.

Instruments that contain a Trigger Bus interface can generate controlled test pulses to the device and synchronize events between instruments by listening to start and stop signals. The test computer can access any of the bus lines through the TimeMaster Pulse Clock. The standard test system dc meter also interfaces to the Trigger Bus.

MEASURE BUS

The Measure Bus, represented in figure 19, allows different instruments to access the meter system. Rather than internal A/D converters in each instrument, a high-speed, high-accuracy meter in the system accesses each instrument via the Measure Bus, providing a cost-effective solution with no impact on test time. For instruments so configured, the Trigger Bus controls when an instrument is connected to the Measure Bus and when the meter strobes the signal on the bus.

MODULATION BUS

When running power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) tests on analog and mixed-signal devices, this bus routes ac instruments to modulate V/I supplies to determine if the device can reject ac signals.

The Modulation Bus provides a 180 kHz bandwidth interface for many of the instruments in the system. The bus is a shielded, differential pair of signal wires that allows multiple instruments to be modulated from a source. Thus, multiple device pins can be modulated simultaneously as required in some crosstalk testing. Individual pins can be modulated as well, to determine device rejection characteristics. The performance on

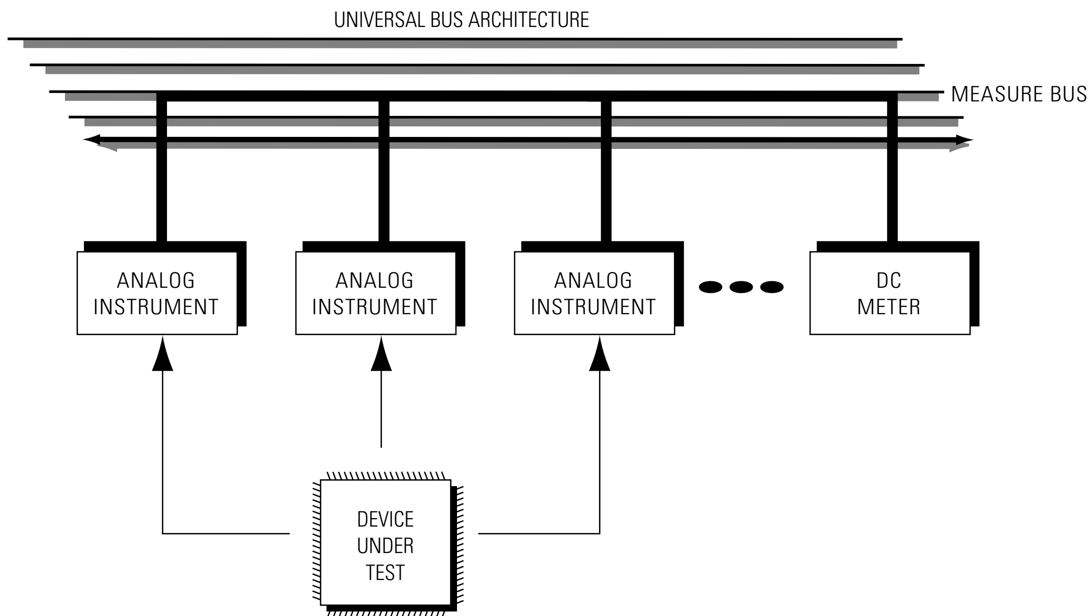


Figure 19
Universal Bus Architecture measurement bus allows shared metering.

any particular pin is limited by the characteristics of the modulated instrument.

TEST HEAD ANALOG DISTRIBUTION SYSTEM (THADS) BUS

The Test Head Analog Distribution System (THADS) Bus is an ac matrix that runs between each of the analog instrument channel cards in the test head. THADS is a shielded differential bus that allows an instrument to access multiple device pins. Also, if a device pin requires different types of instruments in order to perform all required tests, the THADS bus can be used to deliver the instruments to the device pin.

For example, if a device has multiple input pins to an on-board A/D converter, the tester analog source can be accessed through the THADS Bus to each input pin. This capability eliminates the need for the user to build a complex relay matrix to deliver the source to each device pin on the device interface board.

Dual Computer Architecture

The A585/A575/A565 series of test systems uses a dual computer platform to meet the demands of mixed-signal test. Dual SPARC® computers are used to provide maximum throughput. The dual computers process the additional calculations necessary for final test results and instrument setup changes, Ethernet and local disk drive communications. The dual computers communicate with each other over an Ethernet link.

One computer interacts with the user and the network providing test program development support, data analysis, management of program loading, and data transfers during testing.

The second computer runs the test program without interruption from the outside world. This maximizes throughput and provides repeatable test times for predictable test capacity, which is very important to ensure production schedules.

The SPARC user computer from Sun Microsystems provides the following set of features:

- microSPARC-II processor 57 SPECint92; 43.7 SPECfp92
- 32 megabyte standard memory, expandable to 256 megabyte
- 1.5 gigabyte standard disk drive, expandable with up to 2 gigabyte
- Ethernet controller
- RS232/RS422 serial port
- A high resolution 1562 x 900 17 inch graphics terminal with mouse

The second SPARC is the test computer, which has the following set of features:

- microSPARC-II processor
- 32 megabyte standard memory
- One RS232/RS423 serial port with optional expansion available
- Optional IEEE interface

The A585/A575/A565 also contains a high-speed array processor to perform all DSP calculations. The test computer sends a list of calculation instructions for the array processor to operate on multiple sets of data. While the array processor performs those tasks, the test computer continues to execute the test program, virtually eliminating the DSP execution time. This pipeline approach is possible because the array processor has its own large data memory to store all the data needed for calculations.

The array processor used on the A585/A575/A565 is the Mercury MC860 processor, which has 4 megabytes of memory, expandable to 16 megabytes. It performs 80 M floating point operations per second and can operate in either single or double precision modes. Devices that contain 20 bit resolution sigma-delta converters require double precision operation to avoid introducing mathematically generated noise to the test results.

COMPUTER NETWORKING

All Teradyne device test systems can be networked directly via Ethernet and to each other, as well as to simulators and other equipment. All systems use the standard TCP/IP protocol. Additional communications interfaces are supported by the software environment for control of external equipment such as handlers and probers. These interfaces include:

- Parallel interface
- RS232 interface
- IEEE interface communication

SUN ETHERNET NETWORKING

A585/A575/A565 series hardware and software tools allow you to reach the market 40 to 70% faster than other test systems. Furthermore, 70% of test program development can be performed off-line at a stand-alone workstation using IMAGE™ software. To support this large amount of off-line test program development, the A585/A575/A565 series offers Ethernet networking. See figure 20. This network feature supports the following functions:

- Test program development
- Engineering and characterization data analysis
- Pre-production test program file library management
- Complete data analysis

NETWORKING AND X WINDOWS

The Sun networking capability, in combination with the X Windows windowing standard, provides an even more powerful test development and production environment. Remote locations on a network can be viewed and operated from your local workstation. This can be as basic as examining datalog results from the test floor or as sophisticated as actually operating the test system remotely.

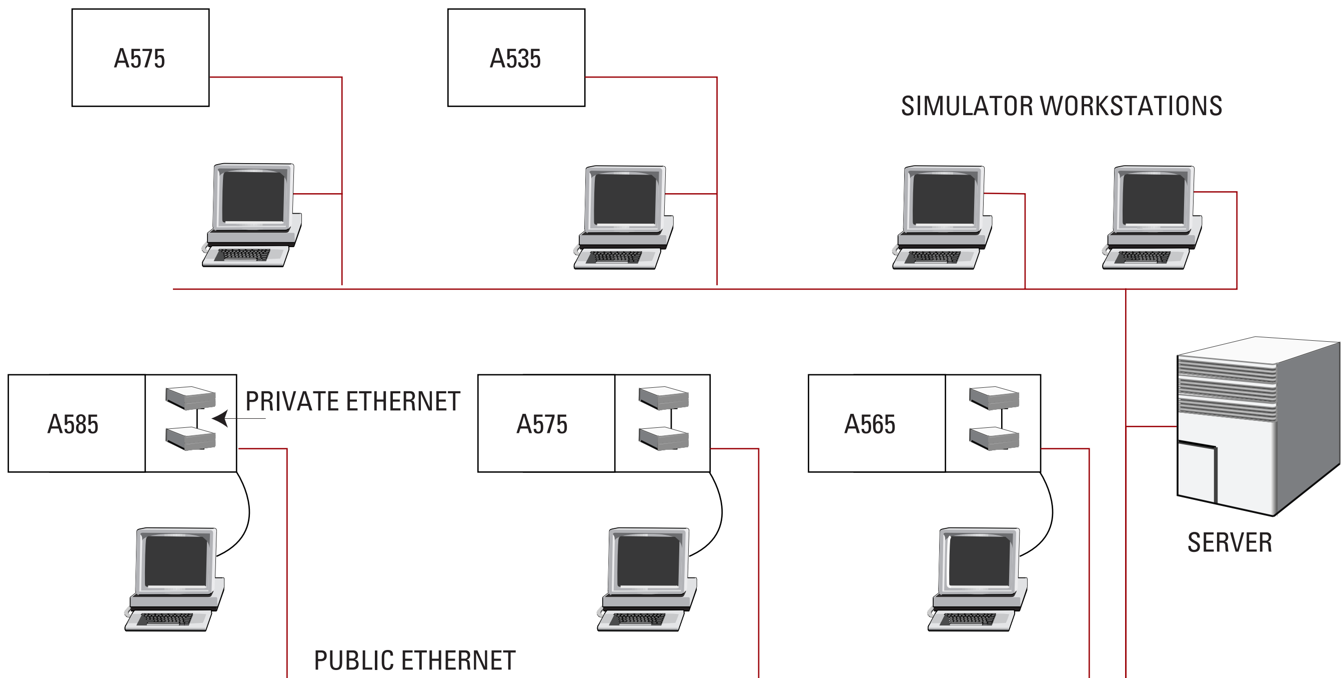


Figure 20
SUN/A500 Family networking

IMAGE Software System

Interactive Menu-Assisted Graphics Environment (IMAGE) software for the A585/A575/A565 series represents an innovative approach to ATE software. IMAGE software uses the power of the test system's dual computer architecture and builds on the strengths of the UNIX operating system and the C language (both industry standards). An advanced windowing environment using the Sun OpenWindows graphical user interface provides graphics-oriented, computer-aided testing tools that are highly interactive and focused on the requirements of AVLSI testing. The result is a test program development environment which dramatically reduces time-to-market for AVLSI devices.

The computer-aided testing tools provided by IMAGE software for test program creation, debugging, and characterization all use this advanced window system. This powerful combination provides a highly-interactive environment where most commands are executed without typing at the keyboard. Hardware status display windows, for example, use graphics windows to clearly show the state of the test system hardware. This high-resolution graphics window system makes test program development much faster than conventional text-editing, keyboard-oriented approaches.

To further reduce test program development time, all of the documentation for the A585/A575/A565 series, as well as for IMAGE software and its components, is available on-line from Teradyne's IMAGE Answers on-line documentation. Updates of the IMAGE Answers documentation are provided with each release of IMAGE software. See figure 21.

CUSTOMIZED ATE DUAL-COMPUTER OPERATING ENVIRONMENT

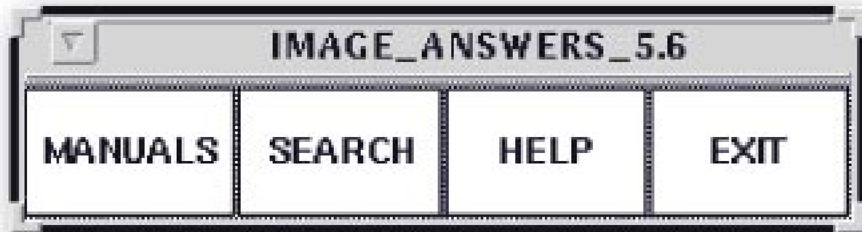
The IMAGE software system customizes UNIX for ATE applications to provide an operating environment focused on the needs of test program development and production testing. This operating environment makes the dual-computer architecture transparent to the user. The user interacts with the system through a single user interface on the user computer. Operation of the test computer is controlled automatically by the operating system.

ETHERNET TCP/IP NETWORKING SOFTWARE WITH NETWORK FILE SYSTEM

The IMAGE test system executive provides Ethernet TCP/IP networking software with Sun Microsystem's Network File System (NFS) to support test program development, data analysis, and characterization on a local network of Sun workstations.

IMAGE PROGRAMMING

IMAGE software corrects the weaknesses of unstructured, tester-oriented languages and conventional compilers and interpreters. The IMAGE test language is device pin-oriented and organized into modular tests and functions. It is a superset of industry



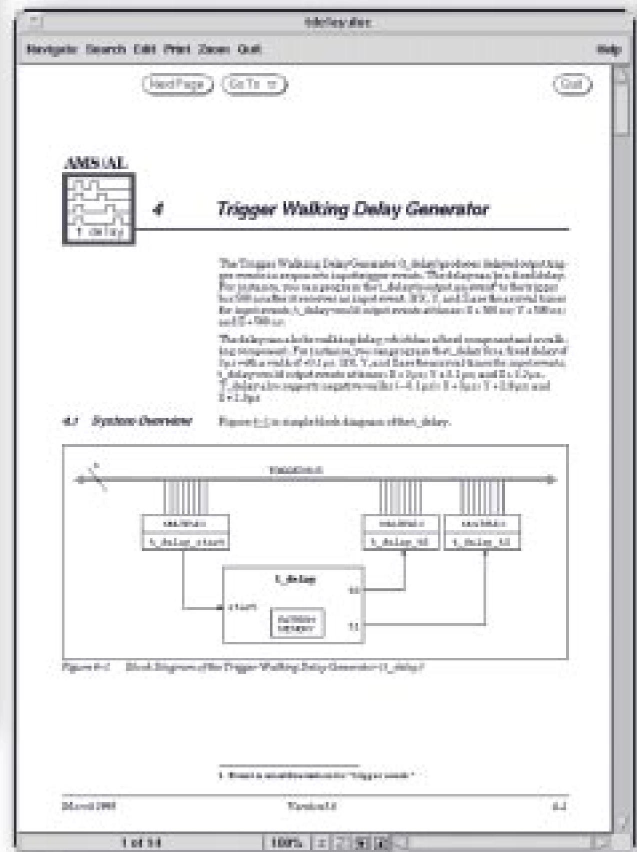


Figure 21
IMAGE Answers on-line documentation

standard C. Its interactive compiler provides very fast turnaround by only recompiling and linking sections of a test program that have been modified. The interactive compiler produces fully compiled code for very fast program execution.

In the IMAGE test language, the entire C language is fully supported. C statements are useful for such tasks as declaring variables, controlling program flow, and performing arithmetic calculations. To control the test system hardware and the DUT, the IMAGE test language provides high-level instrument commands customized for each test system instrument.

Instrumentation Drivers

Each test system instrument has a software driver written in C, an efficient language, for fast execution and high throughput. These software drivers control the test system hardware by implementing the high-level language commands that are part of the test language. A test engineer programs the hardware using easy-to-understand commands such as “set <instrument>” and “start <instrument>.” These commands are translated into instructions for each software driver. (Also see Device Pin Oriented Language, later in this section.)

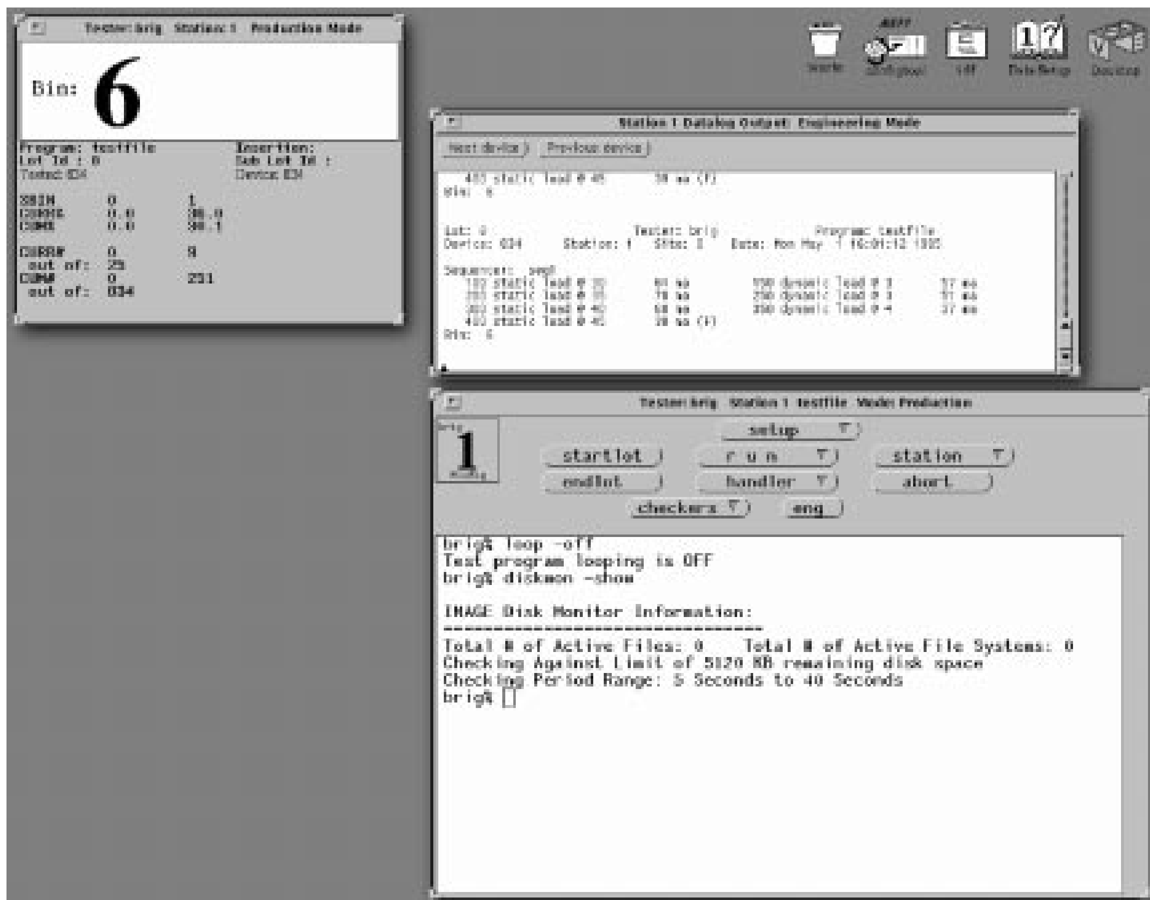


Figure 22
IMAGE production environment

Digital Signal Processing Software Library

Testing mixed-signal AVLSI devices on the A585/A575/A565 series of test systems is done using digital signal processing techniques for characterizing analog ac waveforms and digital signals. A large selection of DSP algorithms including Fast Fourier Transforms (FFT), vector-vector, vector-scalar, and matrix operations is provided. These algorithms run on a 32-bit floating point array processor (operating at 80 MegaFLOPS), for unmatched device characterization and high throughput. The array processor is available with either 4-Megabyte or 16-Megabyte memory.

TEST PROGRAM ORGANIZATION

The structured organization of an IMAGE test program facilitates test program development, debugging, and maintenance. An IMAGE test program is organized in five main sections making programs much easier to understand and maintain:

- Binning Strategy
- Pinmap
- Sequencers
- Tests
- Functions

Binning Strategy

The Binning Strategy section is a software association of soft bins (useful in the summary) and pass/fail determinators to hard bins (sent to handler/prober). This allows multiple soft bins (multiple device grades) to be mapped to a pass condition and multiple soft bins (for yield analysis) to be mapped to a single hard bin. This section also allows the declaration of test conditions such as hot, cold, room, etc., which can be set at program load time.

Pinmap

The IMAGE Pinmap is a software "wiring diagram" that describes the connection between the test system channels and the DUT pins. The DUT pin names defined in the Pinmap are used in the device pin-oriented programming language that is described below.

Collections of pins can be grouped and given a symbolic name — this is typical of bus-oriented digital interfaces. An entry can also be made in the pinmap to check the DIB ID code. This ensures that a program can only be executed if the correct loadboard is installed on the test system.

Sequencer

The sequencer defines and controls the flow of a test program. See figure 23. The main elements of a sequencer are:

- Test name
- Test number
- High and low limits
- Test label
- Pass, fail, and close bin for down-grade binning when multiple binning strategies are implemented for a device type

A quick look at a sequencer immediately shows, as in a specifications sheet, the tests performed, the order of the tests, the pass/fail conditions, and the binning strategy. In contrast, test programs on other testers force you to examine the whole program to understand which tests are performed and to locate the test limits. This makes maintenance of test programs

PIN	NAME	DIB/CONFIG	CHANNEL
pinmap={			
1	"D1"	dib:h_7	hsd50_rcv:1,
2	"Ain"	dib:14a1	plfsrc_hi,
3	"Vcc"	dib:27a1	dutsrc,
4	"GND"		local,
.			
.			
};			

Table 1
Example of actual syntax for device pinmap

extremely difficult, especially by people who did not write them.

Unlike other test program software systems, IMAGE test programs can contain multiple sequencers. One sequencer may be used for hot test, another for cold, probe, QA, etc. All can be contained in one test program, simplifying program maintenance.

Tests and Functions

Functions are the basic building blocks of a test program. A function is an independent executable section of a test program which is similar to a subroutine or procedure in other languages. A test is a special type of function designed for use in a device test program. Tests are called from the sequencer where their order of execution is defined. A test contains statements to control the hardware and to return test results to the sequencer. This structured organization allows interactive development and debugging of test functions since only modified tests must be recompiled and linked to the rest of the test program.

Device Pin-Oriented Language

A test engineer, when developing test programs, thinks about the device being tested, not the tester. The IMAGE test language uses high-level commands that are device pin-oriented, not tester-oriented. This approach allows great flexibility and makes programming much easier. On the A585/A575/A565 series, device-to-system connections are programmed once. After this is done, instruments connected to the DUT can be programmed using device pin terminology. For example, to program

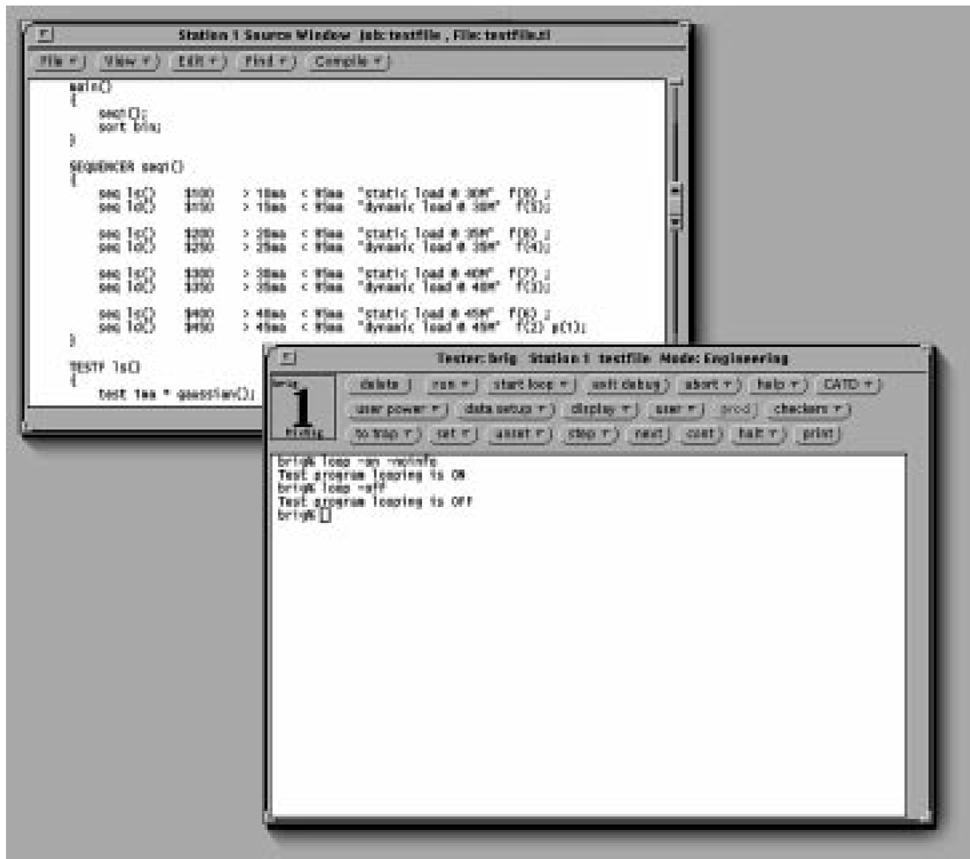


Figure 23
IMAGE station window with sequencer

the DUT source connected to the device pin named “Vcc” to 5 V requires the following programming:

set pin=Vcc src
v=5volts;

Notice that the name or number of the source is not needed in this programming statement. Only the name of the pin (Vcc) need be programmed.

Contrast this approach to a tester-oriented language where commands must refer to test system resources. To duplicate the Vcc programming above, a test engineer must search through the test program to find which power supply is connected to the Vcc pin and write a command to control the specific hardware used. All this makes programming difficult and maintenance even worse, adding to the time and resources required for program development.

The device pin-oriented language supports the dc instruments, ac instruments, and all digital channels on the A585/A575/A565 series system hardware using high-level commands. This is key to the IMAGE software environment providing full support for parallel device testing.

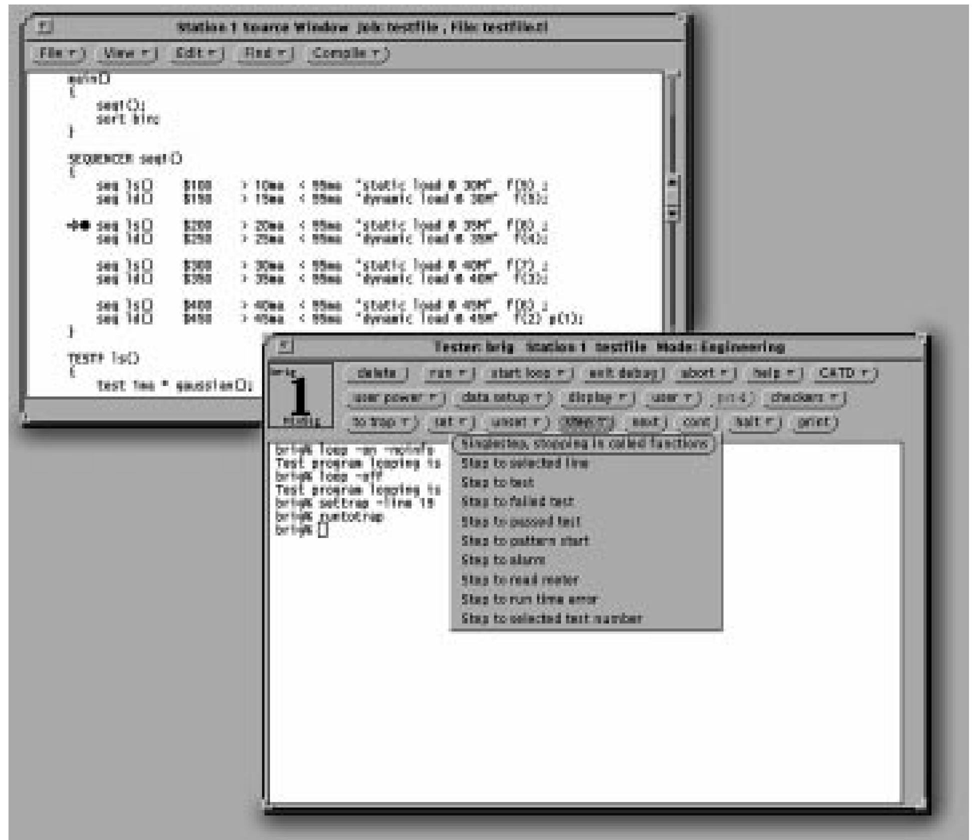


Figure 24
IMAGE station window with trap and menu

INTERACTIVE TEST PROGRAM EDITOR AND DEBUGGER

IMAGE software is the ideal tool for developing test programs. It includes editing and debug tools. See figure 25. When you log onto the tester, a station window opens. This represents the user's interface to the test system. Each station window is divided into several sub regions. For instance, the station window in figure 23 has a command region and a button region. Any command can be executed by selecting that command using the mouse ("clicking on" it) in the button region. Each command can also be typed in the command region instead of using the mouse.

Text from IMAGE Answers, such as programming examples, can be copied directly into the test program. This helps eliminate typing errors and further enhances the power of the on-line documentation environment.

Source-level Debugger with Breaktraps

After loading a test program, source-level debugging is begun by selecting the debug command. A test program source region opens automatically and a breaktrap can be selected using the mouse at any time, indicated by a graphic stop sign (figure 24).

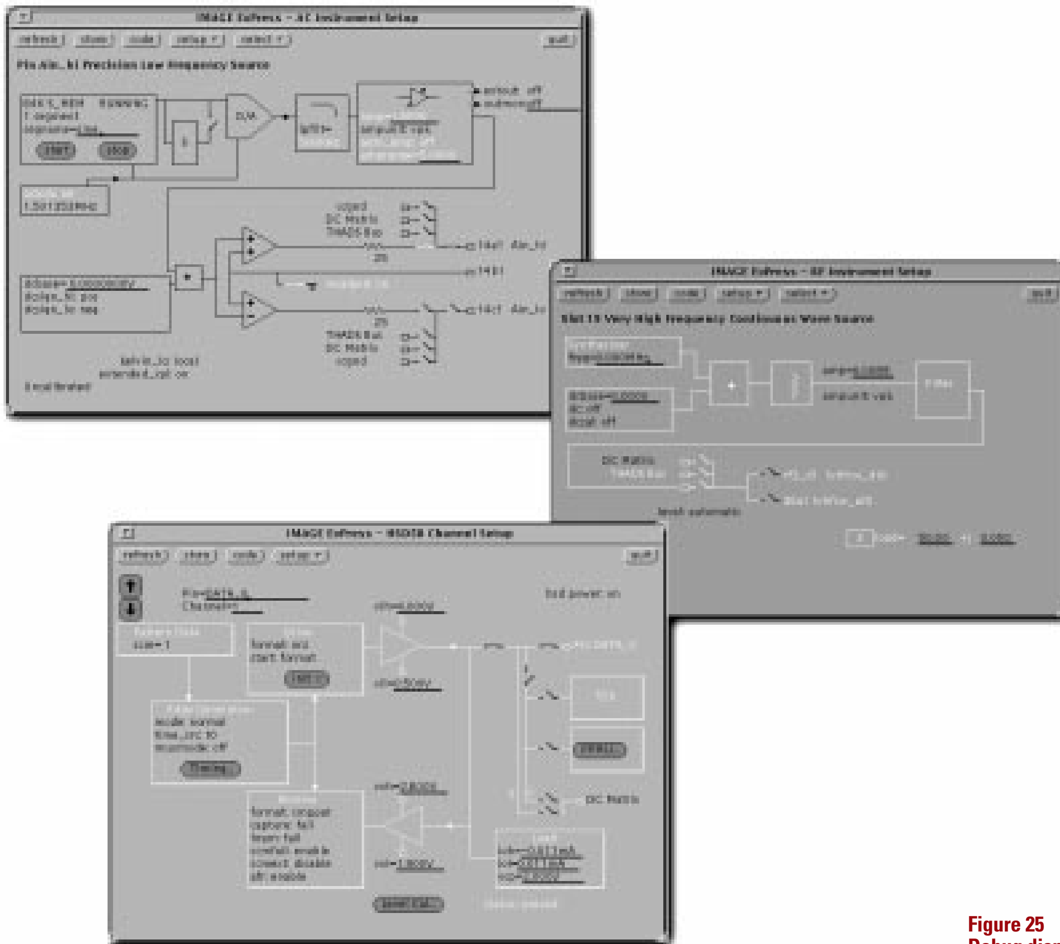


Figure 25
Debug displays

Incremental Compile for Fast Turnaround

After using the editor to modify the test program, the compiler is called using the mouse without leaving the editing environment.

The IMAGE compiler performs incremental compilation, which means that only the sections of the test program that were modified are compiled. This technique provides fast turnaround. For example, if you only change one test, you can compile and be ready to try out your changes in less than two seconds. This two-second turnaround time does not vary with the size of the test program. In addition, the compiler outputs efficient, fully-compiled binary. There is no throughput penalty for interactive response time.

Immediate Statement Execution

Immediate commands are very useful for experimenting with the test system hardware or with your device. A dedicated window is provided for immediate statement execution. You can type any language statement or multiple language statements and have them incrementally compiled and executed immediately to temporarily affect the state of the test system hardware. You can even execute an entire function or file from this window. A single-line immediate command executes in one second or less providing very fast turnaround. It is very easy to edit an old immediate command or insert it into your source program. The immediate window has editing capability built into it and keeps a history of all immediate commands you have executed.

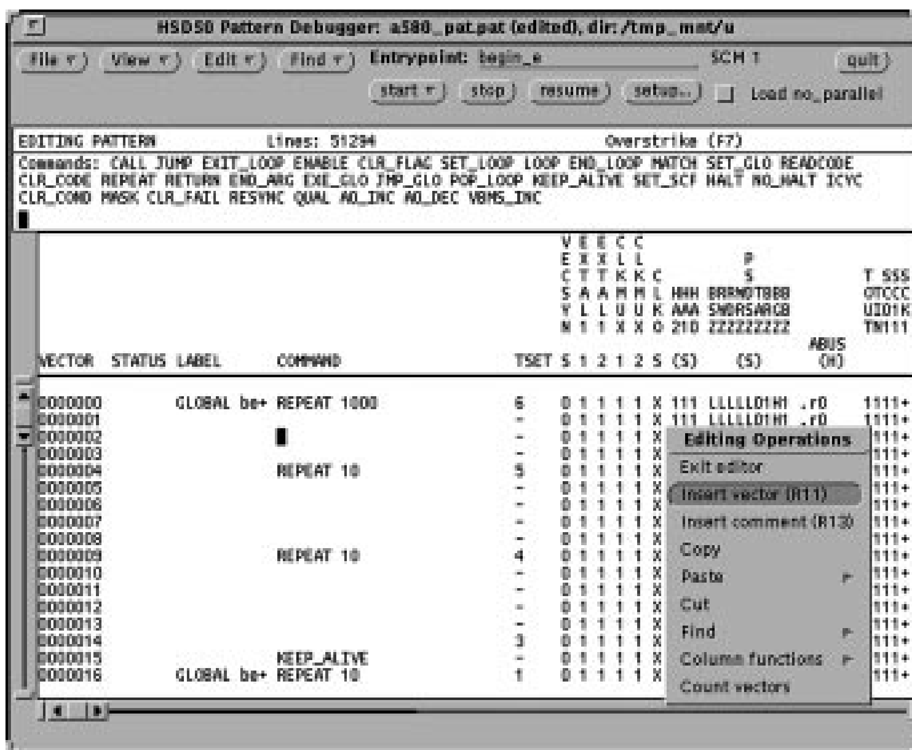


Figure 26
Pattern debugger showing column operation

INTERACTIVE DIGITAL AND ANALOG DESIGN AND DEBUG TOOLS

IMAGE software includes many interactive, graphics-oriented tools specifically designed for development and debugging of digital vectors, digital signals, and analog waveforms.

Digital Pattern Editor and Debugger

The IMAGE Digital Pattern Editor and Debugger provides a powerful development environment customized to the task of creating, modifying, and debugging high-speed digital patterns in the shortest possible time. This editor allows you to easily specify the device pin digital state data, vector control and Mixed-Signal Microcode control instructions on a per-vector basis. The Pattern Editor displays the pattern in a spreadsheet-style. Edits are incrementally compiled on-the-fly for very fast turnaround. Patterns can be debugged on the hardware without leaving the editor environment. See figures 26 and 27.

When you complete a pattern editing session, your pattern is saved to a binary file which can immediately be loaded into pattern memory. No separate off-line compile step is required. The long compilation times usually associated with digital pattern development are eliminated. The incremental compile capability of the Digital Pattern Editor makes pattern development much faster than on competitive systems.

Another key feature of the Pattern Editor allows you to select a device pin or group of pins and change their state data without affecting other pins defined along the vector. These column-oriented editing functions

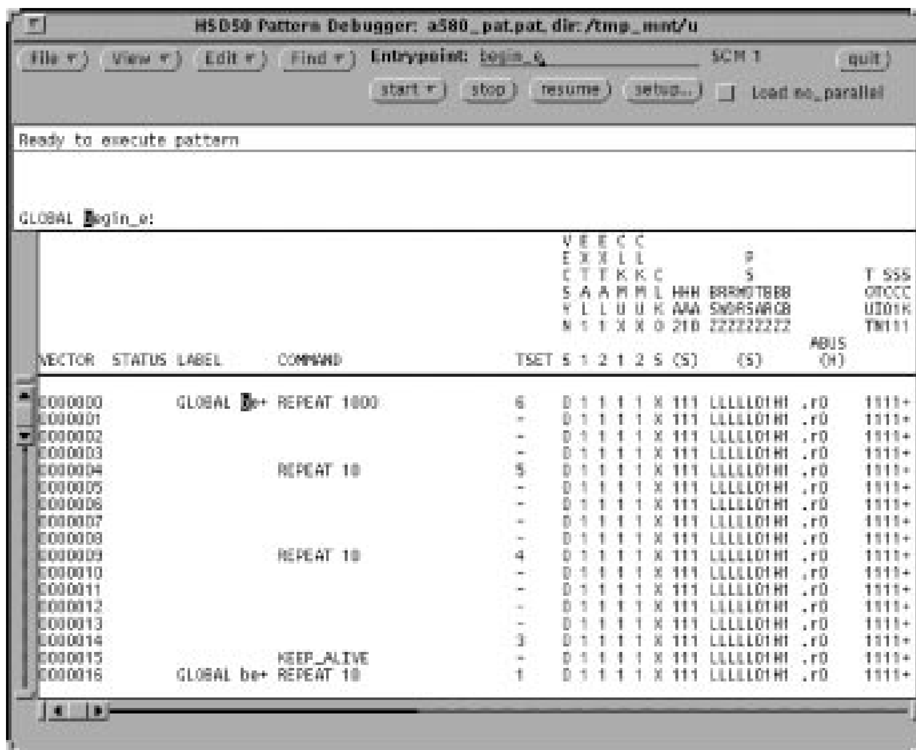


Figure 27
Digital pattern debug window

allow you, for example, to change the state for one pin along the whole pattern with a single mouse operation. A pin or group of pins can be selected and the data moved up and down by some offset without affecting unselected pins.

Digital Pattern Advanced Logic Analyzer

The Digital Pattern Advanced Logic Analyzer (figure 28) can display digital patterns at run-time. Depending on the format used, the selection of timing sets and channel state data, the “shape” of the waveform going out of the digital driver and the expected windows are displayed in the time domain.

The Digital Pattern Advanced Logic Analyzer includes many features found in advanced logic analyzers such as pre- and post-triggering, functions with “compression” of data using different radices such as hexadecimal, and a trace function to allow easy debug of complex random patterns with conditional branches. The Logic Analyzer can also “digitize” waveforms using the comparator on the digital channel card. This technique allows users to see exactly what the waveform looks like at the comparator and then to adjust the comparator strobe timing to get accurate and repeatable test results.

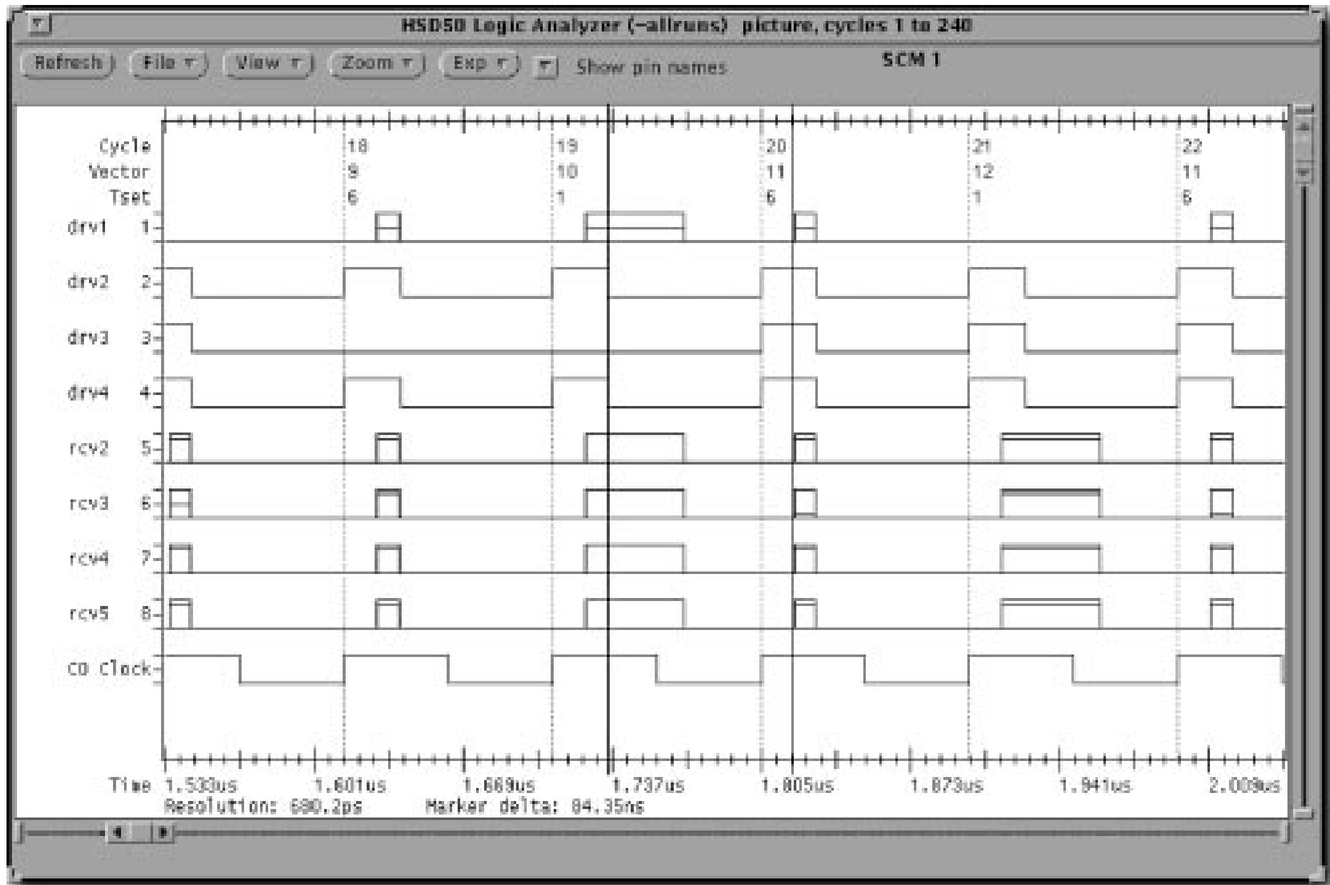


Figure 28
Digital Pattern Advanced Logic Analyzer

Digital Waveshape Tools

A major enhancement to the programming environment for the high-speed digital subsystem is the suite of Digital Waveshape tools (figures 29 and 30).

The Spec Table (figure 29) allows digital specification and test parameters like setup/hold time to be captured in an electronic "spec sheet." Then the Timing and Levels Tool, called DIGW, uses equations to describe timing relationships in terms of these device specifications. This is a very powerful and flexible alternative to describing the thousands of timing

specdisp dir/u/digw

File ▾ View ▾ Edit ▾ Find ▾ Debug Quit

Select ▾ spec_set2 @ spec_file @ a580_specs.speca

Symbol	Item	Description	Value	Min	Max
Tc	1	cycle	50ns	25ns	200ns
tst	2	tstate	25ns	25ns	100ns
ts34	4	EXTAL high to CLK>	14ns	2.1ns	10ns
offset	6	Dummy shift of e >	12ns	0ns	20ns
syncval	7	Used to help find >	7ns	0ns	20ns
ts35	8	CLKO high to ABU >	15ns	7ns	28ns
ts37	9	CLKO high to TSZ >	50ns	30ns	120ns
ts39	10	CLKO high to TAZ >	2.5ns	5ns	20ns
ts40	11	CLKO high to BSZ >	0ns	−20ns	20ns
ts41	12	TAZ valid to CLKO>	10ns	25ns	100ns
ts42	13	CLKO high to TAZ >	10ns	8.5ns	34ns
ts43	14	CLKO high to DBU >	12ns	7ns	28ns
ts44	15	CLKO high to DBU >	−8ns	−20ns	20ns
ts45	16	DBUS in valid to C>	12ns	30ns	120ns
ts46	17	CLKO low to DBUS>	−7ns	7.5ns	30ns
ts47	18	CLKO low to RDZ. >	10.5ns	−20ns	20ns
ts48	19	TSZ hold time fro >	13ns	10ns	40ns

Read done.

Figure 29
Digital waveshape tools – spec table window

relationships that are required in the digital portion of a test program. This also dramatically simplifies the development of characterization routines.

Analog Waveform Display

For creating, debugging, and modifying analog waveforms and digital signals, an interactive window-based tool is available to display signals in the time and frequency domains. The display window (figure 31) accepts data from multiple sources such as

digw dir:/u/digw

File View Edit Find Debug Quit

Select a580_eset_data @ a580_eset_data.diga

Eqset Comment Basic Timing

Pinname	Eset	Fmt_drv	Fmt_rcv	Edge	Equation	Value	Commen
CLKO	1	off	cmppat	r1	offset		
				r2	CLKO.r1@1+5.1ns		
ABUS	1	off	cmppat	r1	offset+ts35		
				r2	ABUS.r1@1+offset+ts47		
DBUS	1	nrz	cmppat	d0	0ns		
				d1	offset+ts45		
				d3	dbusio		
				r1	mask		
				r2	mask		
BSZ	1	off	cmppat	r1	offset+ts35		
				r2	Tc+offset+ts40		
RWZ	1	off	cmppat	r1	offset+ts35		
				r2	RWZ.r1@1+offset+ts47		
RDZ	1	off	cmppat	r1	offset+tsrd1		
				r2	Tc+offset		
WRZ	1	off	cmppat	r1	offset+RDZ.r1+tswr1		

Figure 30
Digital waveshape tools – timing table window

digitizer capture memory, any waveform segment, data array and files. Button commands are available to control the displayed area. Smooth and zoom functions are available for a more flexible display.

Using this tool, complex waveforms can be created, debugged, and modified. The display functions are equivalent to a digital oscilloscope and a spectrum analyzer using digital signal processing techniques. The tool can also perform automatic waveform analysis for faster characterization turnaround.

Graphic Instrumentation Status Displays

The A585/A575/A565 series contains a variety of instruments, each of which has many programmable features. To provide detailed information, each instrument has its own graphic display in a separate window. At any time, you can open or close a graphic icon of an instrument for a detailed examination of an instrument's status. Instrument setup changes can be made by "clicking on" the graphic display; by pressing one button, the IMAGE commands that program the setup can be inserted into the program.

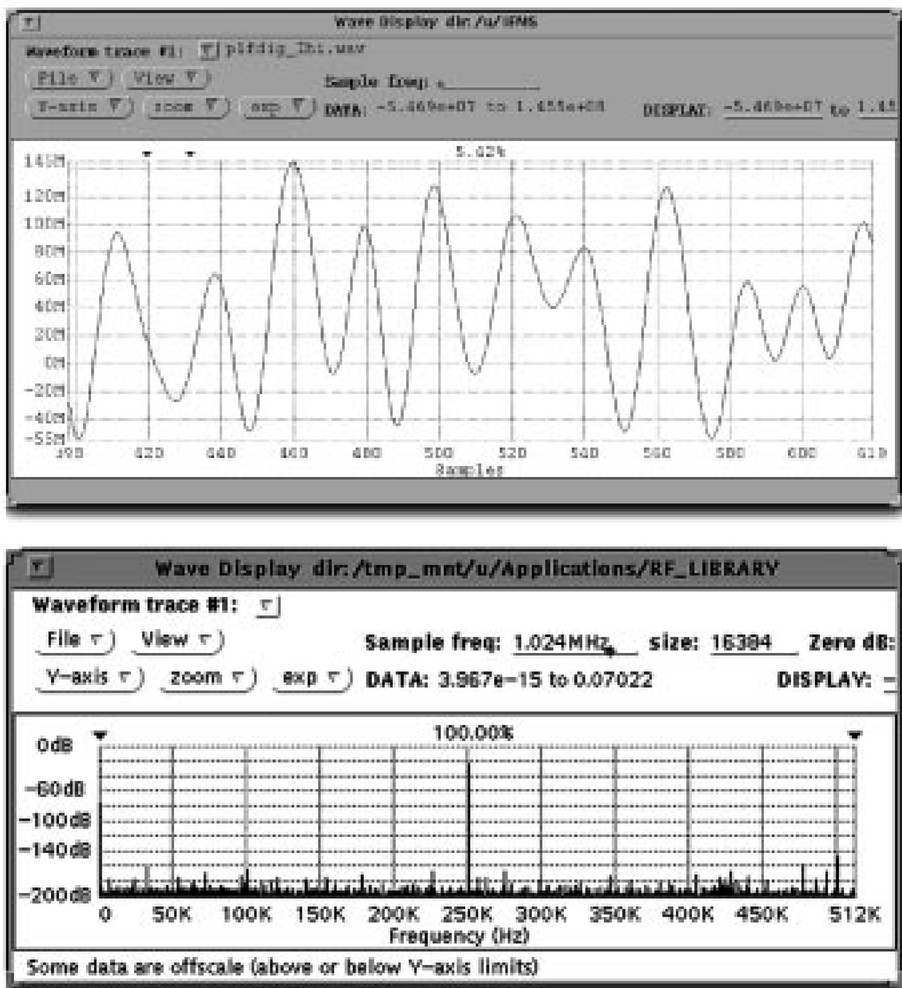


Figure 31
Waveform displays for time and frequency domain

DATA ANALYSIS AND CHARACTERIZATION SOFTWARE

Datalog Reports

IMAGE software provides powerful data collection and analysis tools. Data collection can be set up during characterization using IMAGE software. Some datalog functions can also be controlled by statements in the test program. Datalog parameters include:

- Sequencer name
- Test number
- Test name
- Test value with pass/fail information
- Test limits
- Binning results

Summary Reports

While testing devices, the A585/A575/A565 series performs real-time automatic collection of test results, and, at any time, partial summary reports can be displayed. At the end of a lot, a final summary report is available, which includes:

- Number of devices tested
- Bin categories with total number of devices
- Full report of failure history

Real-Time Histograms

On-line, real-time histogram and correlation software is available and can perform analysis concurrently with device testing. Snapshot results and analysis can be displayed using

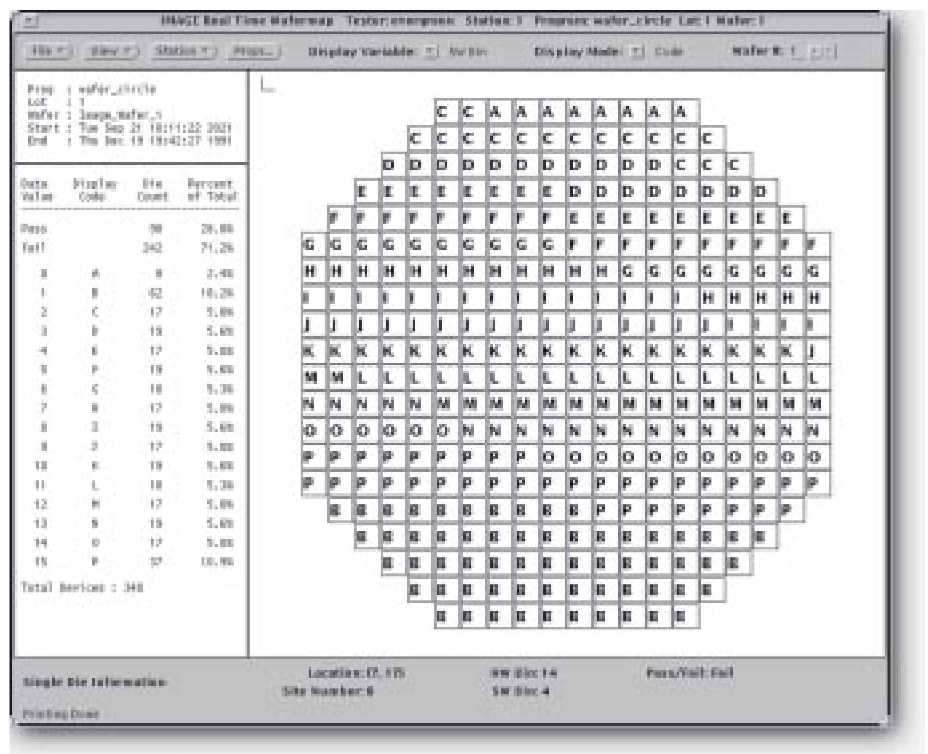


Figure 32
Wafer map

statistical analysis tools. Figure 33 shows a histogram analysis display.

Digital and Parametric Shmoo Plots

Shmoo plot parameters can be entered and then executed from the test program or during debug (figure 34). Tracking parameters are possible on any axis, and mouse editing allows easy development.

3-D Shmoo Plots

The A585/A575/A565 series also offers an optional software product with three-dimensional Shmoo plotting. This powerful mixed-signal analysis package allows two parameters to be varied while a third parameter is measured. The resulting "surface" can provide months' worth of characterization data in a matter of just a few minutes, and the results are all on one graphic display (figure 35).

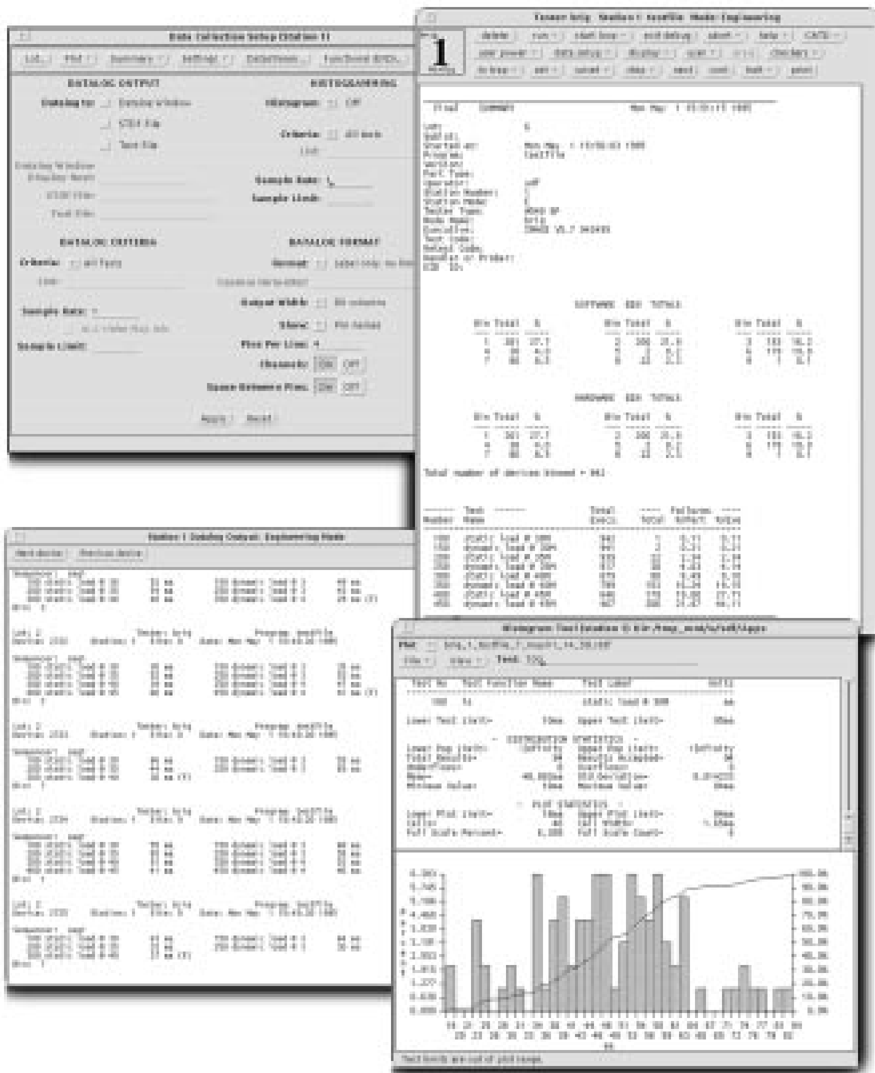


Figure 33
Data analysis tools – histogrammer, datalog, summary report

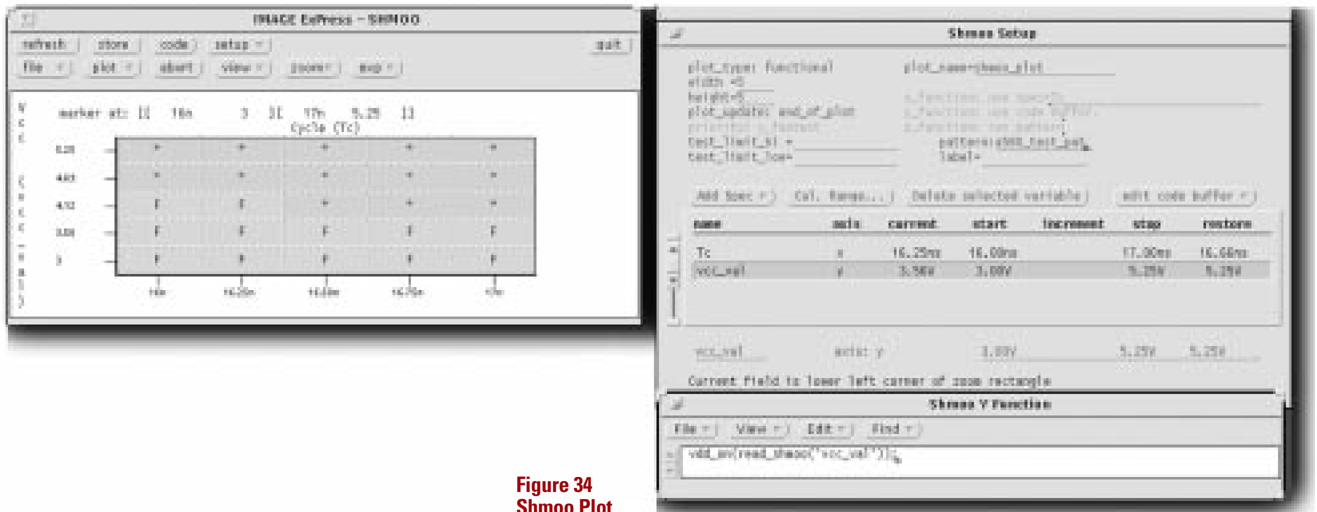


Figure 34
Shmoo Plot

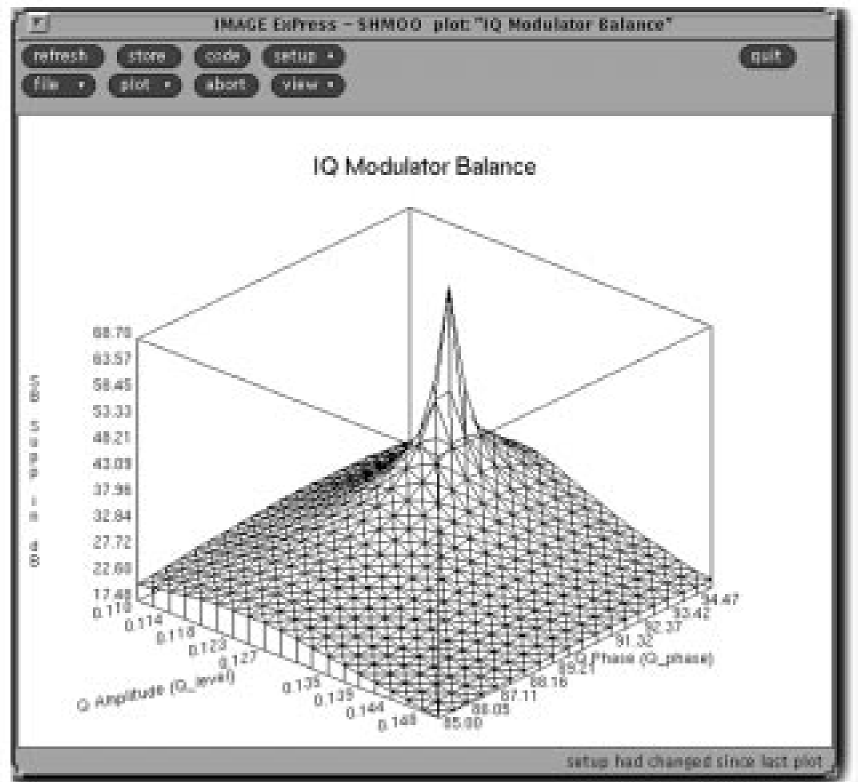


Figure 35
3-D Shmoo Plot

COMPUTER-AIDED TEST DEVELOPMENT

Additional IMAGE Software Tools: IMAGE ExPress™ and ProGen™

Optional software tools are designed to reduce test development time by automating key steps in the creation of test programs. The initial set of tools includes:

- IMAGE ExPress code-producing display (figure 36), which allows test instrument setup by simply "pointing and clicking" at a graphic display using a mouse. Then at the press of a button, the program code to produce the instrument setup can be generated and inserted into the test program.
- The ProGen test database management system, which simplifies the management of symbolic code test modules and test program assembly.
- Device testing libraries in the ProGen format, which provide proven test methods and waveform data for a family of devices such as converters, video, telecom, and disk drive devices.
- Analyzer tools, which provide a family-specific signal generation and analysis environment that simplifies device characterization as well as program development and simulation.

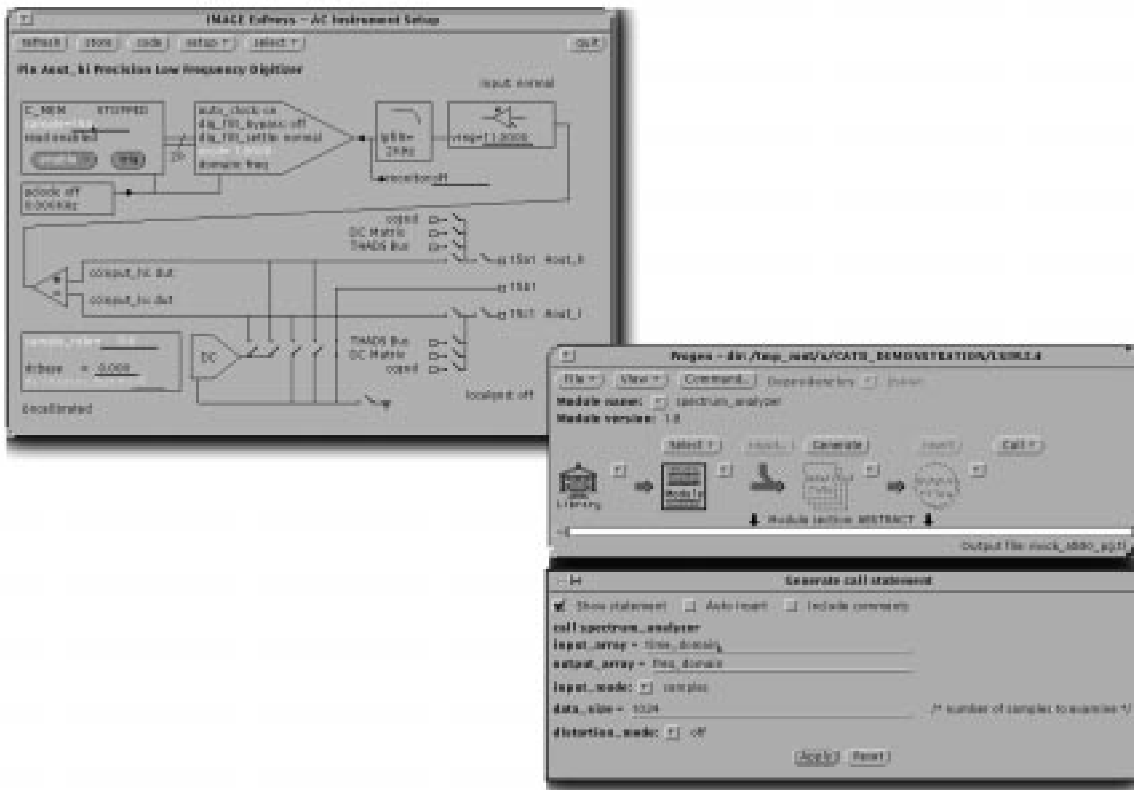


Figure 36
CATD tools - ProGen, IMAGE ExPress

Device Test Libraries

Dedicated tools are available to help the test engineer when working with industry standards for:

- Telecommunications devices (such as filter/CODECs, ISDN and digital cellular)
- Consumer devices (such as PAL, NTSC, or SECAM)
- Industrial and peripheral devices (such as disk drives and converters)

These tools provide the ability to generate and analyze signals required to perform functional testing of mixed-signal devices. Also included are test program functions that allow you to easily implement functional tests in your test program (figure 37).

Sun Stand-Alone Workstation and Tester Simulation Software

In the past, test programs were developed using stand-alone systems and software tools with limited performance. The A585/A575/A565 series offers an off-line stand-alone

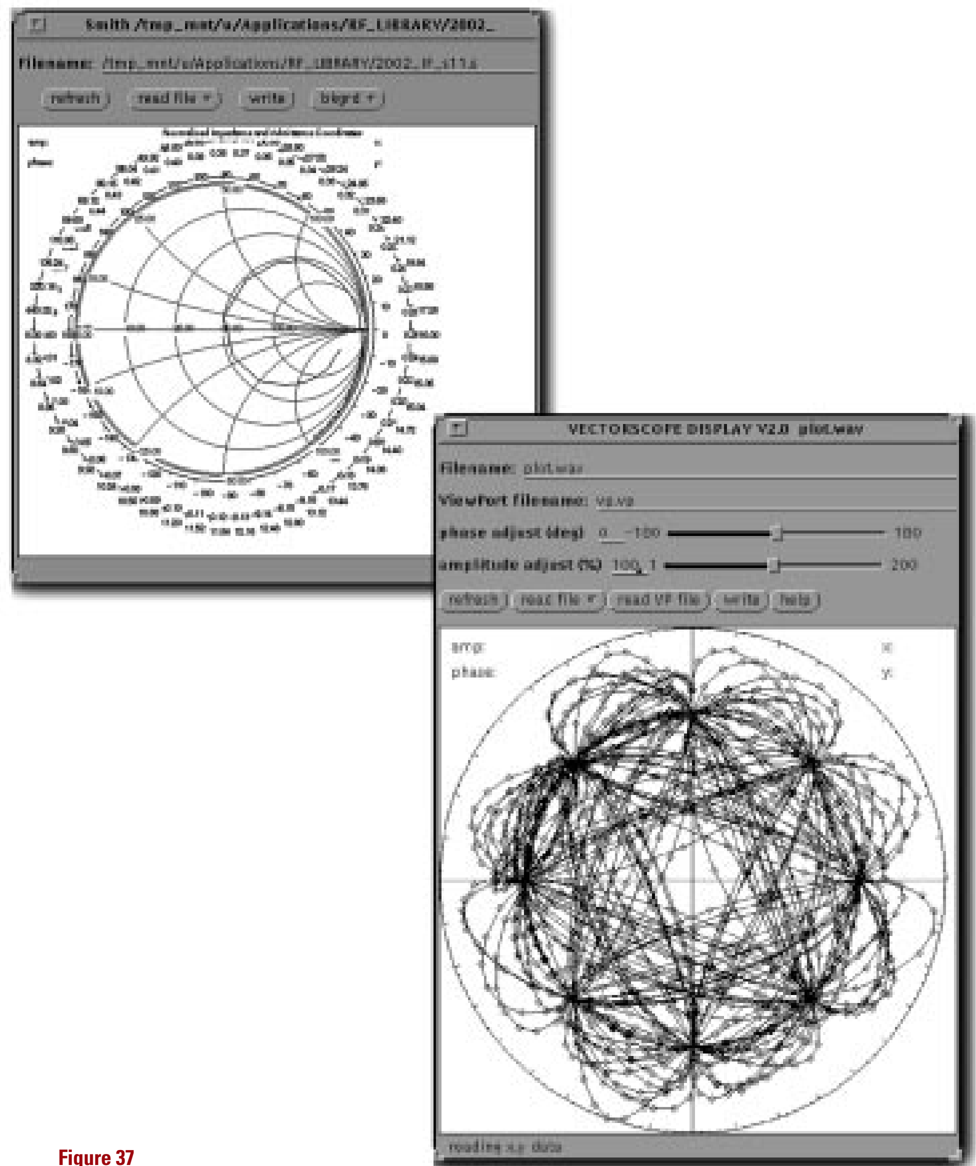


Figure 37
Smith Chart and VectorScope

workstation with full tester simulation software. This workstation uses the same IMAGE software environment and the same Sun computer as the tester. Thus, test engineers working at an A585/A575/A565 series workstation or at the test system use the same commands for creating, editing, debugging, modifying, and maintaining test programs. This reduces test program development time and shortens the learning curve.

Using the Stand-Alone Workstation While Testing

Developing test programs on the Sun off-line stand-alone workstation saves you time in two ways. First, using IMAGE software with its computer-aided software tools reduces program generation time by 50%. Second, in a typical production environment, about 70% of test program development can be performed on the Sun off-line workstation and 30% at the tester. This means that the stand-alone workstation reduces the time required at the tester for development (including editing, debugging, and maintenance) by up to 70%.

All A585/A575/A565 series hardware is simulated on this workstation and some device responses can also be easily simulated using data files for checking and debugging the processing path of the test program. For example, digitized ac output data stored in the capture memory can be simulated using a known array representing device output with known defects. This data can be analyzed using the test program DSP algorithms supported by the Sun stand-alone DSP library. This method allows you to debug the processing path of the test program without using tester time.

Digital Simulator Software

Digital patterns may come from CAE, CAD, or simulation tools with data post-processed or handwritten. One of the most critical aspects of debugging these patterns is predicting any timing violations that could reject good devices and pass failing ones.

The Sequence Control Module controls random sequences of vectors that may be conditional to external events and to pass or fail conditions. Jump operations, for example, may have different destination addresses that may, depending on a timing set used, violate test system timing specifications. The Sequence Control Module simulation software makes sure that timing hazards do not exist. This software tool runs on the stand-alone Sun workstation using tools available with IMAGE software. When used with IMAGE software, it can save as much as 40% to 60% of test program development time for complex new devices. In fact, writing test programs for such devices may become impossible without such computer-aided testing tools, just as designing such devices has become impossible without CAD and CAE tools.

Simulation-Based Development Using IMAGE ExChange™

The goal of Test Simulation is to reduce the impact of test development on the time to market for new ICs. This can be achieved by enabling test development to begin earlier and in parallel with IC design. Test Simulation uses simulation technology to reduce the amount of debugging that must wait for the availability of device silicon and test time on the production test system. See figure 38.

The test engineer develops the entire test package using a complete Test Simulation environment. IMAGE ExChange, which is at the center of this simulation environment, communicates the state of the simulated test system to a design simulator which supports behavioral models of A585/A575/A565 series instrument models, DIB and DUT. See figures 38, 39 and 40. This combination creates the ability to actually debug the interactions of the test program, test instrumentation, DIB and DUT.

The benefits of this approach include:

- Test development independent of first silicon
- Test development independent of available test system time
- Reduced load on production ATE
- Additional IC design verification via test involvement

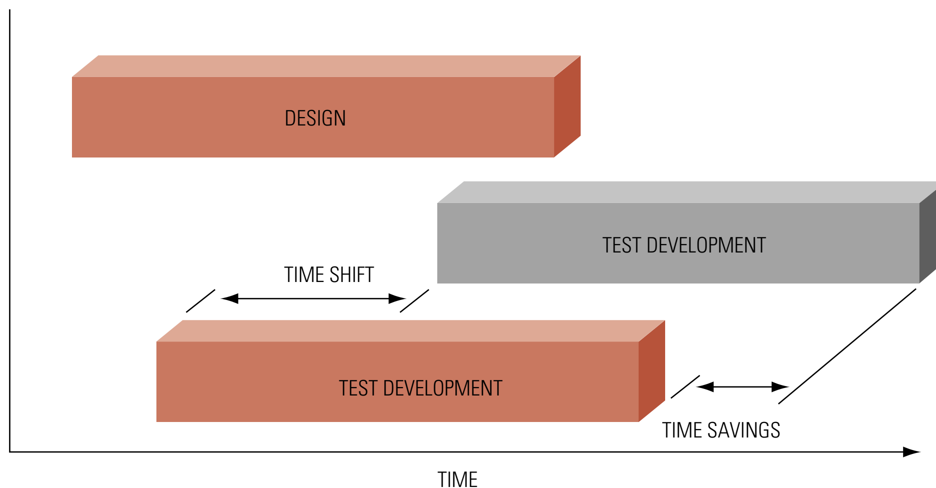


Figure 38
Test development – today vs. tomorrow

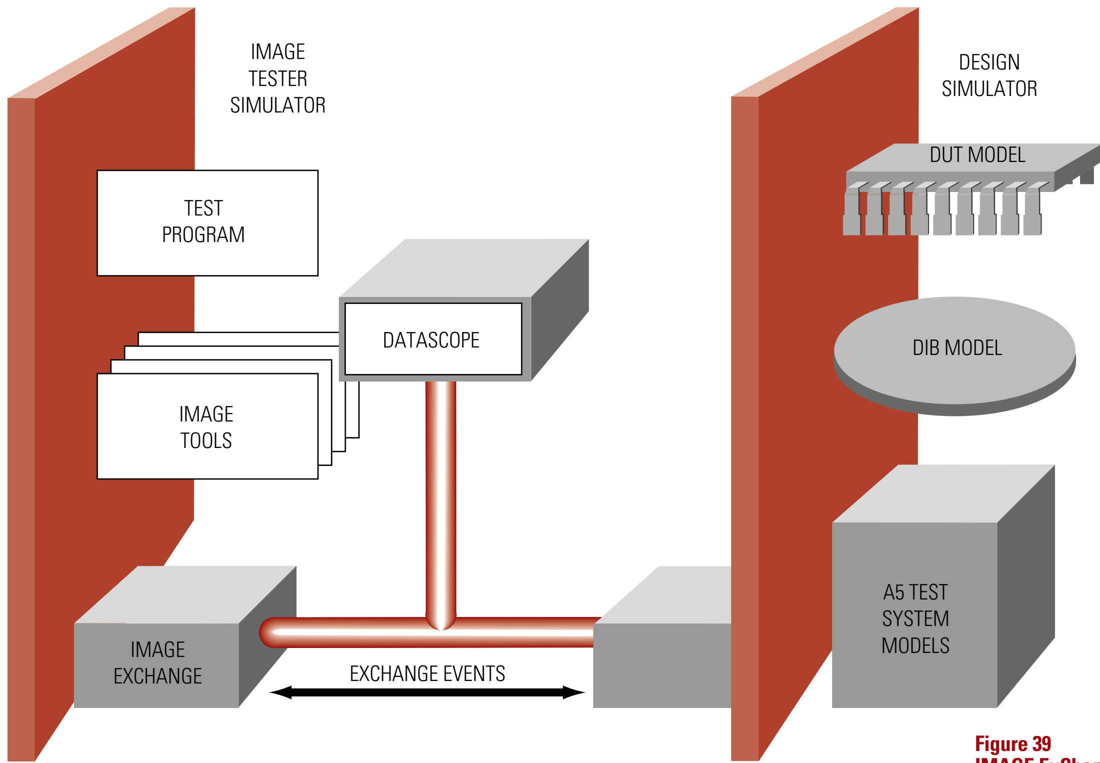


Figure 39
IMAGE ExChange

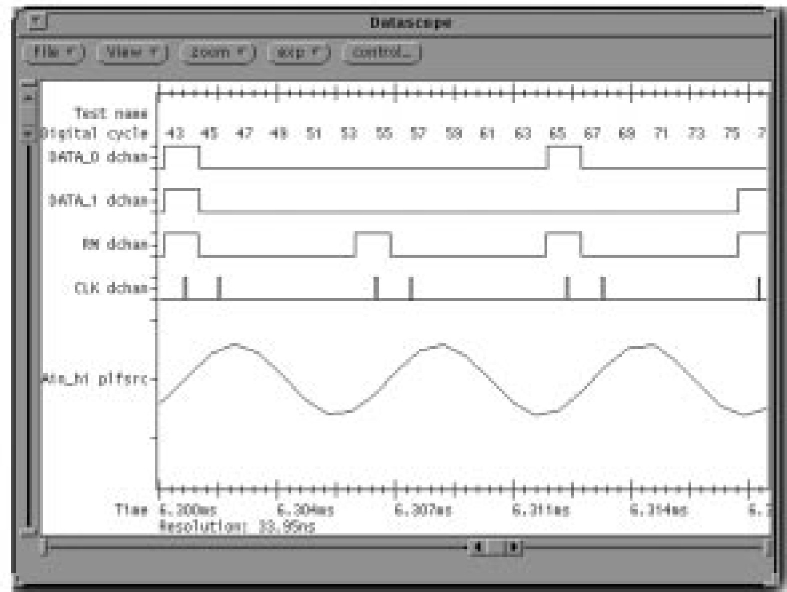


Figure 40
DataScope

INSIGHT ANALYSIS SOFTWARE AND OTHER TOOLS

To analyze test data, Teradyne offers the Insight Analysis product line. Each Insight Analysis product delivers innovative graphical solutions to specific engineering and operations problems. The Insight graphs show thousands of pieces of information in a single view, helping engineers to:

- Identify problems which may have otherwise been missed
- Save weeks of engineering time by reducing thousands of separate analyses to a single graph

The Insight Analysis product line can help meet engineering and operations challenges at each stage of the development and production cycle, from first silicon to daily production.

Design Insight

Design Insight is used to characterize device performance over an unlimited number of operating conditions and equipment variations. When a device is tested over a set of different temperatures, voltages, or other parameters, Design Insight provides the tools for completely characterizing the effect of each setting, in isolation or in combination with other conditions. With this information, design engineers can modify simulation models and improve their design methodologies. The reports can help product engineers understand the performance of first silicon so they can set manufacturing guard bands.

Design Insight offers high-level “roadmap” reports, which can show how every test responds to changes in each of the variable testing conditions. Once these reports have quickly isolated any problems, the many low-level graphs provide detailed charac-

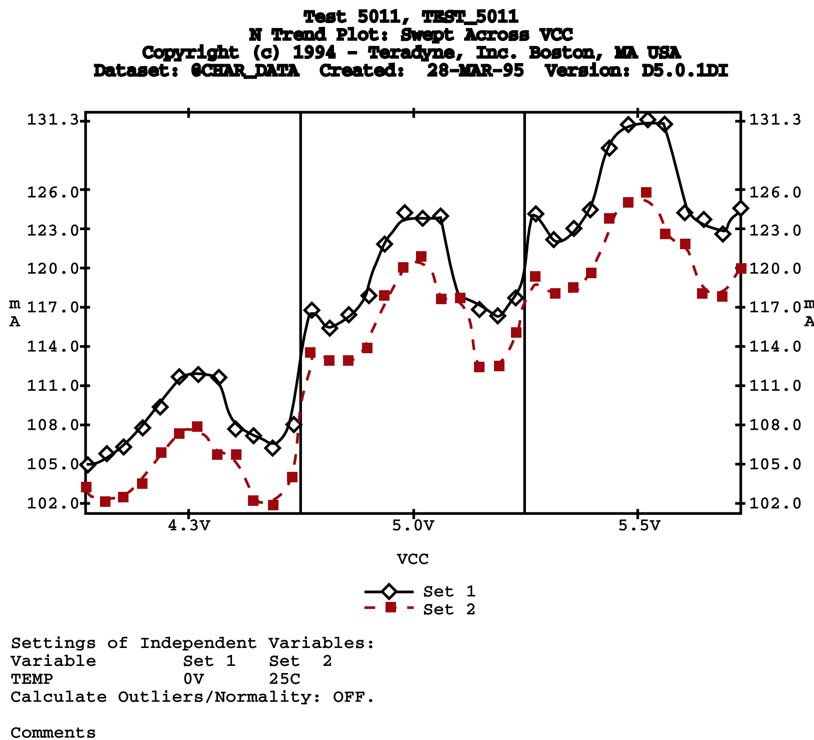


Figure 41
Design Insight – This N Trend Plot shows the effect of changes in voltage (VCC) and temperature (the two trend lines) on the test results for each device. One use of this report is to help isolate which operating conditions have a significant effect on a device's behavior.

terization of the device. For a sample report, see figure 41.

Test Insight

Test Insight helps engineers develop test programs that maximize yield and minimize test times. In the development of a test program, Test Insight can identify critical parameters that may lower yield and can help verify that the test program is testing the device correctly. It can predict yields before the release to manufacturing, to assist in operations planning. For a mature product, Test Insight can reveal ways to optimize test times in order to maximize test system capacity.

Some Test Insight reports visually summarize information about all the tests in the test program, indicating tests whose low Cp or Cpk predicts a low yield, or highlighting tests whose distribution approaches or crosses the high or low test limit. Another useful report shows for each test, significant lot-to-lot variations in mean and standard deviation, thereby uncovering repeatability problems between processes. Test Insight also offers detailed analysis of single tests, such as device trend plots and histograms, to drill down on problems discovered by the high-level reports. For a sample wafer map, see figure 42.

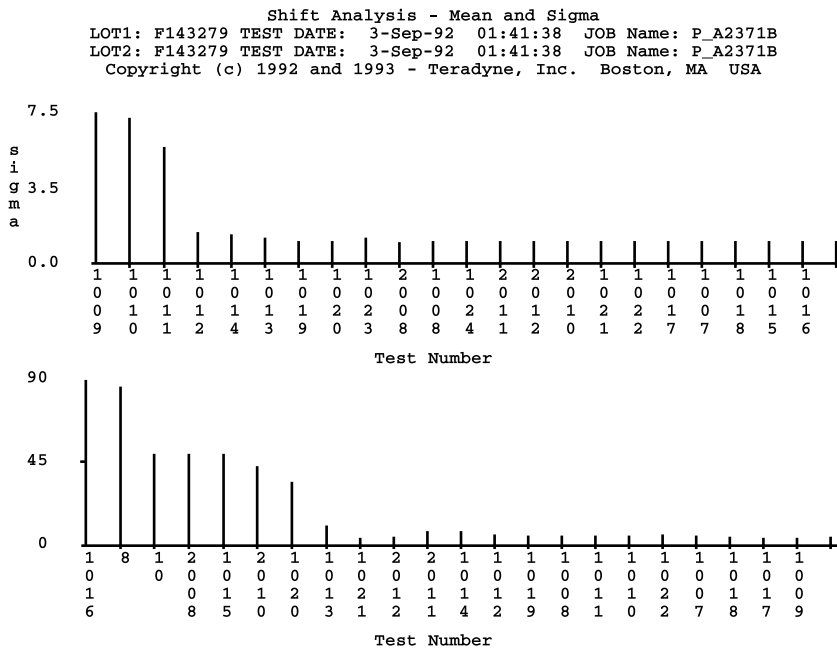


Figure 42
Test Insight – The Mean and Sigma Shift report compares two lots and shows which tests display the greatest shift in the standard deviation and the mean. This information is valuable for determining measurement differences after a change in operating conditions or between process splits.

Wafer Insight

Wafer Insight organizes wafer manufacturing data into graphic reports that make wafer processing problems immediately visible. Other reporting packages, such as Test Insight, can offer valuable views of wafer data. However, to find problems that are specific to wafer processing, it is necessary to tie parametric test results back to actual die locations on the wafer. That is the power of wafer maps.

Wafer Insight offers a complete suite of wafer maps. Traditionally, wafer maps have consisted of ASCII representations of bin sorts. Wafer Insight goes beyond such bin maps to include maps based on pass/fail results and measured parametric results for a single test. Its ASCII maps are complemented by several full-color graphic maps of bins and parametric results. In addition to its maps of single wafers, cumulative maps of a stack of wafers can locate distribution problems, mask defects, and other problems that are common to the same die location across many wafers. For a sample plot, see figure 43.

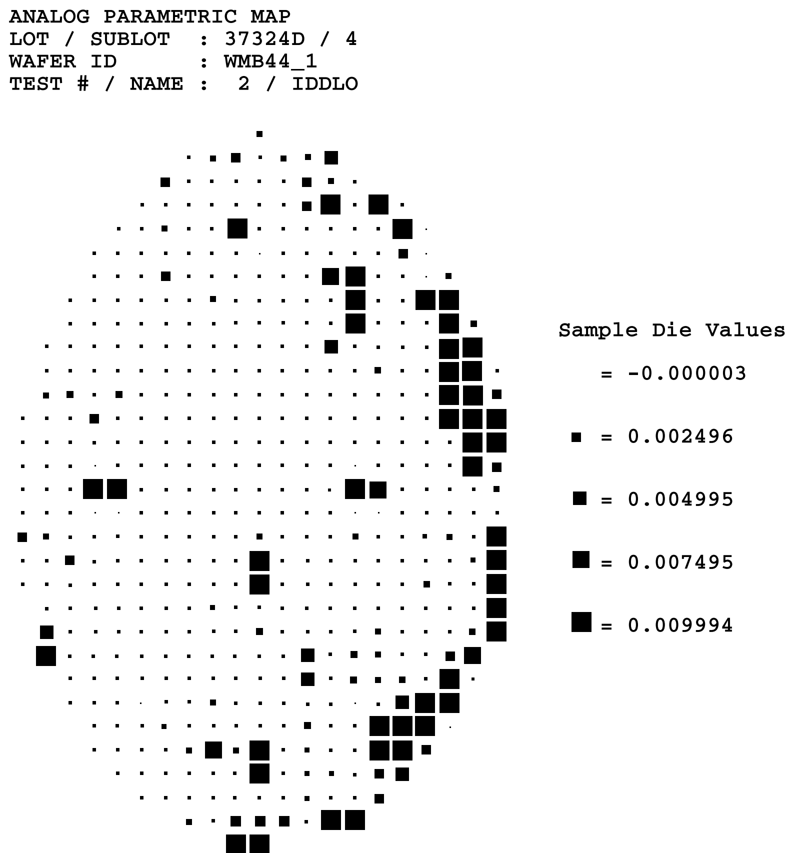


Figure 43
Wafer Insight – The Analog Parametric Map shows each die as a box whose size is proportional to the parametric value of its test result. On this map, higher values are found on the right edge of the wafer, suggesting that there is non-uniformity in the wafer processing.

Production Insight

Production Insight is most useful when a device is in production and operations management wants to look at yields and test results over a long time interval. Production Insight summarizes the vast amounts of production data into trend plots, pareto plots, control charts, and other reports. These high-level views let the engineer stand back and look for trends in a sizable population, instead of being distracted by aberrations that may appear only in a single lot.

The Production Insight control charts can alert the production floor manager when a process is out of control. Other Production Insight reports can then help analyze the out-of-control process. Trend charts can indicate whether yields are rising or falling. Bin paretos can show what kinds of failures are occurring over several lots. A yield pareto by site or tester can be used to correlate results from different parts of the test floor. These reports can be used to identify and correct any process problems that arise during production. For a sample plot, see figure 44.

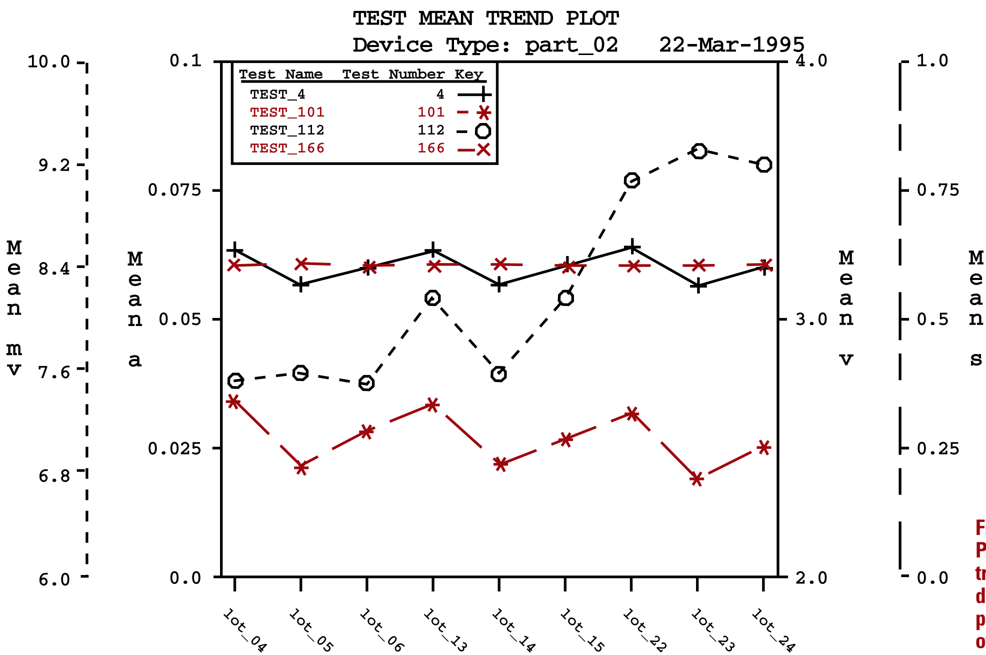


Figure 44
Production Insight – This Test Mean Trend Plot tracks the mean of four tests over several lots of data. Such a report can help identify process problems that may arise over an extended period of time.

Manufacturing Data Pipeline

Underlying the Insight Analysis tools is the Manufacturing Data Pipeline, a complete data architecture for automatically and reliably collecting data from the test floor, and for managing fast, easy access to the collected data. In addition to supplying data to the Insight product line, the Data Pipeline can also be used in the development of in-house analysis tools to provide the low-level data collection and management functions.

The Manufacturing Data Pipeline is designed to handle large volumes of data, and can take as input any data file written in Standard Test Data Format (STDF). Teradyne test systems can directly write STDF files, and data from other test systems is readily convertible into STDF for insertion into the Data Pipeline and eventual use by analysis tools.

Automatic Time & Event Logger

In addition to the Insight Analysis tools, Teradyne offers the Automatic Time & Event Logger, also called ATE Logger. ATE Logger runs directly on the test system, with the goal of making sure that the equipment is used to capacity. ATE Logger automatically time-stamps and records significant equipment events such as initialization, setup, start and end of lot, and maintenance procedures. It also provides for manually reporting equipment failures and repairs and other equipment states. In this way, a log is maintained of all test system activity, both regular and unscheduled.

To make this log useful for utilization analysis, ATE Logger includes a tool that generates reports of the test system activity data. Several graphical reports show throughput, operator usage, test program runs, failure and repair times, and the duration of any test system activities. A comprehensive utilization summary report is also available for periodic overviews. For a sample plot, see figure 45.

In addition, ATE Logger also provides for the automatic transfer of test result data files from the test system to the Manufacturing Data Pipeline system where data is stored and analysis is performed. This connectivity between the test system and the analysis system is one of the most important features of ATE Logger.

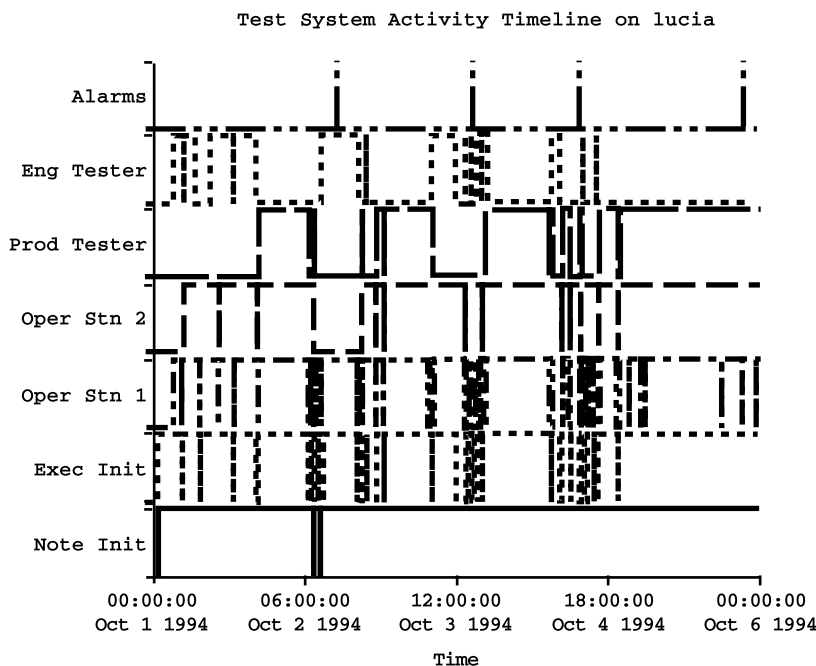


Figure 45
ATE Logger – The Activity Times Report is a timeline that displays the changing state of each selected test system activity. Such a report shows where time is being spent on a test system, information that can help in maximizing resource utilization.

Analog VLSI Digital Test Capabilities

As manufacturers integrate digital designs into system silicon, testing demands increase. In order to meet both signal as well as pattern requirements in these mixed-signal devices, the A585/A575/A565 series contains analog VLSI capabilities as shown in table 2 below. The following pages describe the A585/A575/A565 analog VLSI capabilities.

DIGITAL CHANNEL CONFIGURATION

Architected to support 512 pins, the A585 accommodates up to 192 AVLSI digital pins. (Please refer to the System Configuration section of this document for a summary of the differences among the A585, A575 and A565 systems.) The digital channel consists of two primary boards: the Digital Mainframe board (DMF) and the digital channel card. Both boards are E/MOS designed and both support eight channels. The E/MOS architecture provides a high level of system performance and reliability with maximum function integration.
The ECL components provide speed and accuracy while CMOS technology supports high density logic functions and maintains low power consumption. Because of this technology blend, the A585/A575/A565 systems consume less power and floor space than any other mixed-signal test systems while maintaining high performance levels.
The A585/A575/A565 systems' modular configuration allows easy and cost-effective field upgrades because backplanes and power supplies can be added as pin count increases.

The mainframe supports two test heads. When adding a second head, either at the time of purchase or after installation, channel cards for the new test head are the only necessary add-ons. The test heads are multiplexed, which allows one station to test while the other station indexes the next device. Or, as some customers prefer, one test head can be configured for probe operation and the second for

	A585	A575	A565
Tester per-pin architecture	Yes	Yes	Yes
Pins	192	128	64
Data Rate (MHz)	50/100/200	50/100/200	25/50
Edge Placement Accuracy	±350 ps ±500 ps	±350 ps ±500 ps	±1 ns
Pattern Depth (max.)	1 Meg	1 Meg	1 Meg
Timing Sets	1,023	1,023	1,023

Table 2
Tester per-pin architecture

engineering or handler operation. Each test head, in conjunction with IMAGE software, fully supports multi-site, parallel test. Running with two test heads is a flexible and cost-effective test floor strategy.

MULTIPLE MEMORY ARCHITECTURE: PATTERN MEMORY

As shown in figure 46, the Digital Mainframe board integrates a number of Vector Bus features and contains the pattern memory for logic testing, plus the formatter and timing generator for edge generation. The pattern memory consists of two portions: a 1 Meg x 3 bit/pin Sequential Access Memory (SAM) and a 16K x 4 bit/pin Programmable Random Access Memory (PRAM).

The IMAGE software automatically splits a pattern between the SAM and PRAM. This split allows easy processing of design simulator patterns into A585/A575/A565 patterns, providing maximum flexibility at minimum cost. The split is invisible to the user who sees only 1 Meg pattern memory depth.

The PRAM supports mixed-signal microcodes per instrument per vector, plus vectors that contain pattern microcodes such as start loop, go to, and execute subroutines. In addition, the PRAM supports up to 32K repeat counts, 5 levels of nested loops, and 8 levels of nested subroutines as well as conditional jumps and match mode loops.

In some mixed-signal applications, additional timing and level parameters may need to be modified; and some patterns may require run-time modification due to device uncertainties. The SETS memory can easily reload these values or the test computer can make the appropriate changes.

In traditional test systems, the pattern is interrupted during these modifications. However, the A585/A575/A565 has a 16 vector keep-alive memory that generates a pattern on all the digital pins during setup conditions or pattern memory modification. The keep-alive memory is essentially a second pattern memory that can be entered from the main pattern memory and then, when specifically directed by

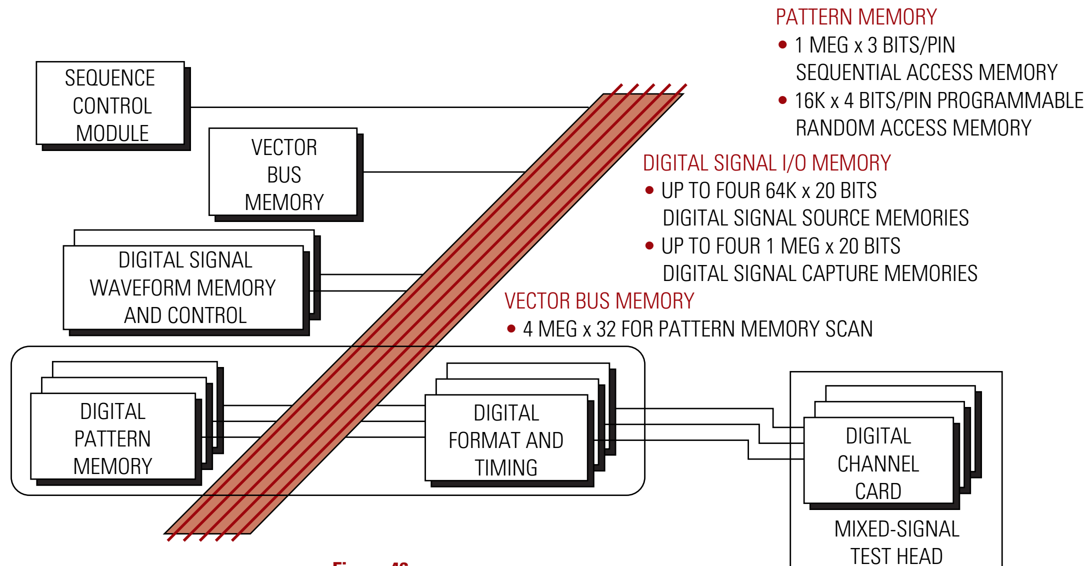


Figure 46
The A585 Vector Bus provides multiple memory types behind each digital pin.

the computer, exited to the main pattern memory for continued testing. Using the keep-alive memory helps maintain device phase coherency and retains device state when reloading main pattern memory or timing information. The keep-alive memory operates at rates up to 50 MHz.

The PRAM provides four bits per pin per vector and the SAM provides three bits per pin per vector, which allows eight pin states to be encoded into the pattern memory. See figure 47. The pattern directly and individually controls those aspects of a pin that change most frequently such as data, direction, compare format, and relevance. This means that pin control resources will be plentiful when post-processing digital device patterns. The normal encoding for the three bit/pin vector is:

- H - Compare to logic high
- L - Compare to logic low
- M - Compare to midband
- V - Compare to valid logic levels
- X - Compare mask
- 1 - Drive logic high
- 0 - Drive logic low
- – - Run time repeat of the previous vector data

The compare to valid pin state is crucial for mixed-signal testing. Analog signals are fed into an A/D converter which generates a series of codes representing the analog waveform. The specific bits are unknown and cannot be truth table compared while testing. However, using compare to valid, the A585/A575/A565 verifies correct logic levels and stores the bits for later DSP analysis.

The repeat state simplifies programming. Pin state data that repeats on successive vectors does not need to be reentered. The run-time repeat pin state is also used in subroutine calls for passing pin states to the routine.

Additional pin state codes include W (waveform), which uses the alternate digital memory, not the digital pattern memory, to source data to the formatter. This function is controlled

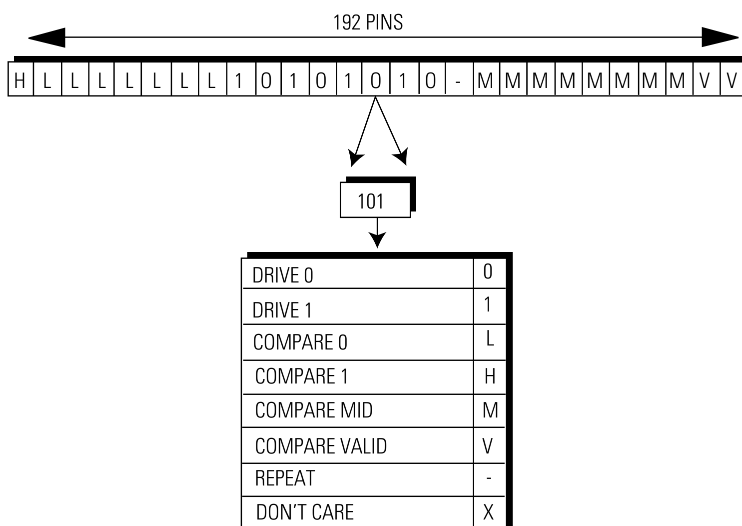


Figure 47
Easy to use mnemonics define the data behind each digital pin.

by the fourth bit in the PRAM architecture. Pin state code I also uses data from alternate memory, but inverts it. Codes R and C take data out of alternate memory and use it for compare. R compares to the data and C compares to inverted data.

Pin states can be reprogrammed to provide other encodings such as dual drive and single cycle I/O, which provide an additional level of flexibility and head room when testing complex mixed-signal devices. Dual drive generates two data values per 50 MHz cycle. The software and hardware recode the bits per pin to represent four combinations of data: 00, 01, 10, and 11.

Single cycle I/O can drive and compare data within a 50 MHz cycle without multiplexing pins. The encoding of the 3 bits located in the pattern data is modified to drive and compare in combinations such as:

- 1 L - for drive one, compare low
- 0H - for drive zero, compare high
- X1 - for mask compare, drive on one
- And other combinations

When pin states are recoded, the 1 Meg data memory is effectively doubled in both the dual drive and single cycle I/O operating modes.

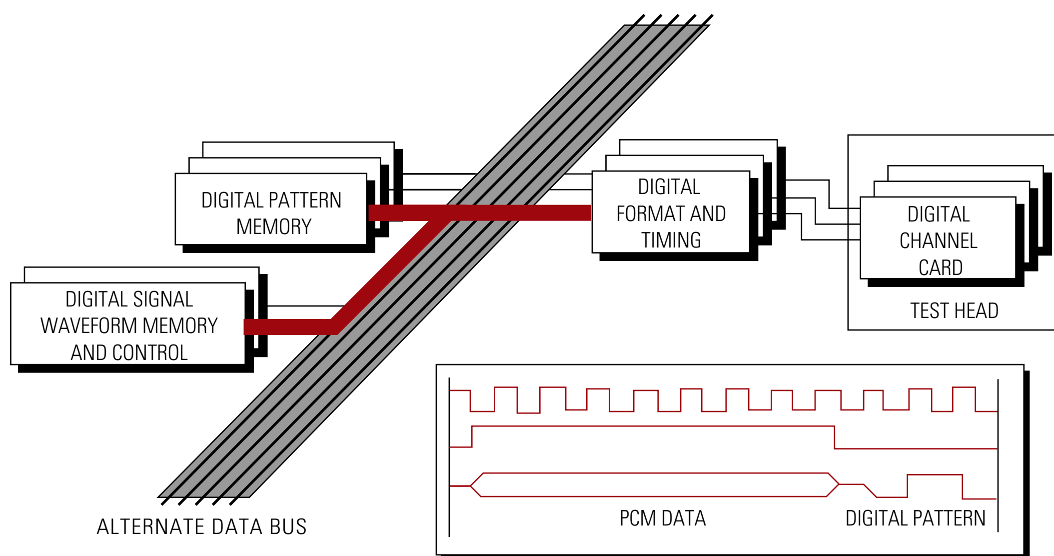


Figure 48
Digital Signal I/O sends and receives the digital representation of analog signals within pattern bursts.

DIGITAL SIGNAL I/O MEMORY

One of the key features of the A585/A575/A565 Advanced Mixed-Signal Test Systems is the ability to provide multisource data mixing that generates and captures digital signals representing analog waveforms.

MultiSource data mixing differentiates the A585/A575/A565 digital capability from VLSI capability and redefines the digital capability as Analog VLSI (AVLSI). See figure 49. Digital signal I/O has three specific functions: a source memory (Smem), a capture memory (dig_cap), and a digital signal controller.

The Smem stores the digital signal representation used when testing a D/A converter. The Smem provides 64K by 20 bits of parallel or serial data storage. The data is usually stored in parallel form to make as efficient use of the memory as possible. Data can be extracted from either the Smem or the standard data pattern memory with an on-the-fly per pin switch operating at 50 MHz. The waveform (W) pin state code, provides the control for selecting the data memory. Components such as ISDN devices require the ability to mix digital signal data representing voice information with pattern data representing framing information and computer data on the same pin in real time. The dig_src contains its own controller that can generate complex waveforms with a series of waveform segments. See figure 49. The controller can REPEAT waveform samples and LOOP on waveform segments and subroutine waveform segments.

The dig_cap captures digital signals generated by components such as A/D converters, which generate codes that are not predictable (due to anomalies such as device noise, linearity errors, gain and offset differences), and then passes the captured data to the array processor where the necessary ac measurement parameters are determined. The dig_cap can capture actual data by using the compare to valid (V) pin state. The comparator simply checks to verify that the device achieves valid logic levels and determines the logic level value stored in the dig_cap. Dig_cap can also capture failed data. This learn mode operation can be used for debugging or for determining the quality of devices that require counting of specific failures or locating specific failures in long pattern sequences. Communications devices such as FAX modems and ISDN devices require this type of testing.

The digital signal controller can change the data from parallel to serial

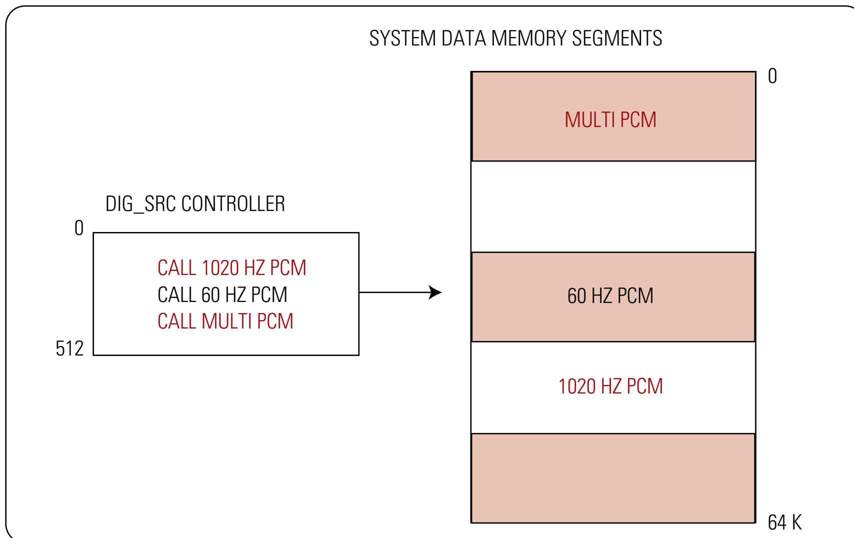


Figure 49
The Smem controller can control up to 512 different waveform segments that can be linked, looped, and nested to generate complex waveforms with a minimum use of memory.

for serial sourcing, or from serial to parallel for serial capture. It can also shift data, handling most significant bit (msb) versus least significant bit (lsb) first formats in real-time. Specific control of bit movement uses mixed-signal microcode such as the SEND, TRIG, SHIFT, STORE, and START commands. These commands efficiently compact the data in memory and can skip vectors within the pattern. They can also send a data bit or data word, depending on whether the operation is serial or parallel.

The digital signal I/O can send serial data at rates of 100 Mbits/second; 20 bit wide words at up to 25 Msamples/second; ten bit words up to 50 Msamples/second; or five bit words up to 100 Msamples/second. It can capture data at up to 50 Mbits/second or 25 Msamples/second for 20 bits; and 50 Msamples/second for ten bits.

With the 32 bit wide Alternate Data Bus, digital signal functions can be assigned to any digital pin in the system for either serial or parallel mode operation. See figure 50. This alternate bus also can source common data from one source to multiple device pins, allowing parallel testing on multiple devices without adding extra memories to the system. Each digital signal system I/O can be connected to the digital pins.

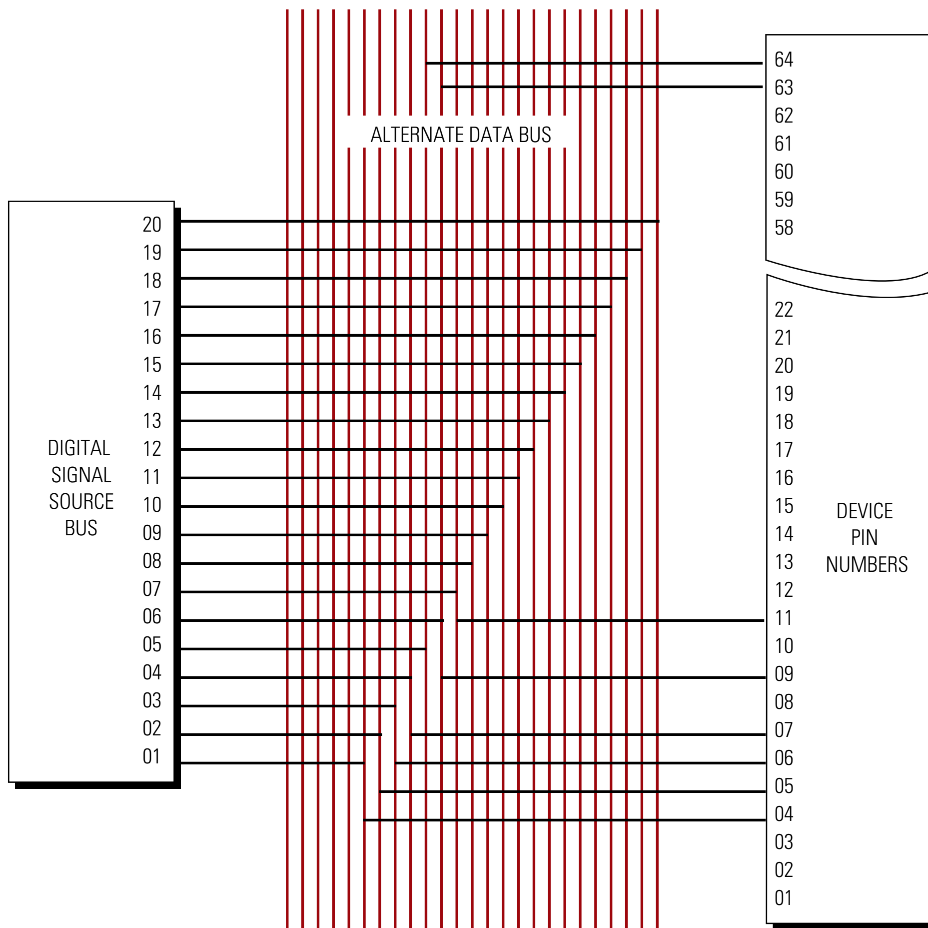


Figure 50
The Digital Signal I/O is programmable to any device pin.

A total of four digital signal I/Os can be configured into the A585 system. Figure 51 shows that each card cage can contain two digital signal I/Os. Either digital signal I/O card cage can be assigned to a block of 64 channels under program control.

The dig_src also can provide compare data to the error and format logic in the comparator channel, especially useful when testing on-board ROM in a device where a serial pin may access the data. If the ROM is 8 K deep and contains 16 bit words, the data pattern memory requires 128 K vectors to test the data. However, only 8 K of dig_src memory is required if the ROM data is stored in parallel in the dig_src and serially shifted via the digital signal controller to the comparator. Since the ROM data is stored in the dig_src exactly as it is stored in the device, only one vector of normal pattern memory is required for testing embedded memories.

VECTOR BUS MEMORY FOR SCAN

Another type of memory, which is accessible to every digital pin in the system, is the Vector Bus Memory for SCAN (VBMS). The VBMS memory is 4 Meg by 32 bits deep, which can support SCAN operations 4 Meg vectors deep and eight SCAN chains wide. The memory is configurable for different depths versus chain width.

The VBMS can also be used to reload PRAM memory. The SCAN operation can run up to 50 MHz rate.

DIGITAL SEQUENCE CONTROL MODULE

The 50 MHz Sequence Control Module (SCM) controls pattern branching and on-the-fly data memory selection. See table 3. The sequence controller executes multiple pattern microcode commands and delivers the mixed-signal microcodes to the analog instruments with up to 16 K memory depth. The A585/A575 can also be configured with dual sequencers, allowing the tester to run both synchronous and asynchronous test under MultiSync TimeGen control.

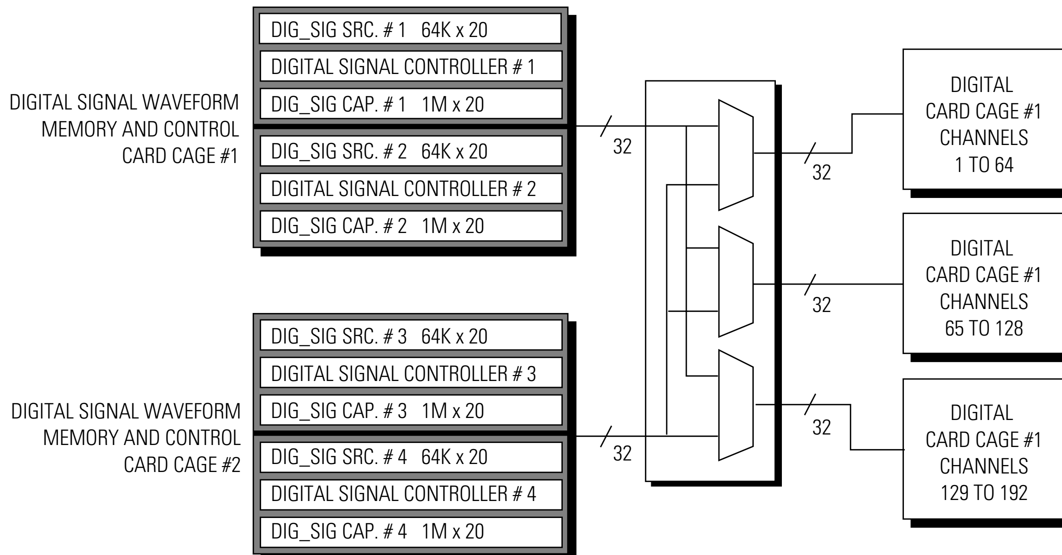


Figure 51
Multiple Digital Signal I/Os are available to each digital pin using the Alternate Data Bus.

PATTERN MICROCODE	FUNCTIONAL DESCRIPTION
- REPEAT <n>	Repeats the current vector n times where n is between 2 and 32K.
Subroutines	
- CALL <label>	Calls a subroutine at the specified label name. Up to eight subroutines can be nested.
- RETURN	Returns from a subroutine.
- END_ARG	Begins the execution of vector arguments that follow immediately after the CALL and is used again to mark the end of the vector arguments.
Pattern Maintenance	
- HALT	Stops pattern execution.
- NO_HALT	Prevents the pattern from stopping if a failure occurs.
- ICYC	Inhibits the SCM cycle counter for that vector.
- MASK	Inhibits failures for the vector specified.
Looping	
- SET_LOOP <n> END_LOOP	Sets the loop counter between 1 and 64K. Up to five nested loops are allowed.
- SET_LOOPi <n> END_LOOPi	There are 3 loop counters, 0, 1, and 2. Only loop counter 0 has a stack depth of three.
- POP_LOOP	Pops the top of the stack unconditionally.
- EXIT_LOOP	Pops the stack and continues execution at the label. Used for premature exit of a loop.
- JUMP <label>	Unconditionally jumps to another vector at the label specified.
- IF (flag) <command>	Conditionally executes a command or multiple commands.
- ENABLE <logic> <flagl,...>	Flags can be logically combined with AND, OR, NOT.
Clearing Flags	
- CLR_COND	Clears flags that are tested in the IF condition.
- CLR_FAIL	Clears all fail flags.
- CLR_FLAG	Clears conditions that have been enabled.
Global Register Addressing	
- SET_GLO	Sets the register to the label given.
- EXE_GLO	Jumps to subroutine label after execution of the current vector.
- JUMP_GLO	Jumps to the label in the global address register.
- READCODE <n>	Read codes can be set by the SCM and read by the test computer. Used to help identify where the pattern is currently executing. The n can be an integer between 0 and 2,047.
- MATCH	Used to define a loop that is looking for a specific sequence of data from the DUT. Allows the tester to synchronize to the device.
- KEEP_ALIVE	Jumps the pattern execution to the keep alive pattern memory for execution there.

Table 3
Pattern microcodes available in the digital sequence control module

Sequence Control Module functions include pattern looping, repeat, jump, match loop, subroutine, and keep-alive control. The sequencer can also execute conditional instructions. For instance, if a condition is true, the instruction is executed; if false, the next vector in the sequence is executed. Combinations of conditions can also be considered with NOT, AND, and OR functions. Conditions include:

- FAIL - Execute command on fail condition
- CPU - Execute command on CPU condition
- VBC - Execute command on Vector Bus condition
- EXT - Execute command on an external condition that has been configured by the user to capture failures or DUT logic levels

The SCM also contains a 1 Meg memory for timing set information so that each test vector can call one of 1,023 different timing sets and repeat counts.

TIMING AND FORMAT

Digital Clock and Data Rates

The A585/A575 are described as 50/100/200 MHz test systems because they can generate 200 Mbit/sec data.

In normal mode, both the sequence controller and the base rate of the tester are programmable to 50 MHz speeds. Some of the methods that allow the tester to go beyond 50 MHz are illustrated in figure 52.

One technique uses a 50 MHz single cycle I/O mode. This means that both drive and compare data can be generated within a 50 MHz or 20 ns vector. The data for each of these states within the cycle is independently programmable. Effectively, this is a 100 MHz data rate mode since two data values can be run within a 50 MHz cycle. Drive and compare positioning within the cycle is interchangeable. In other

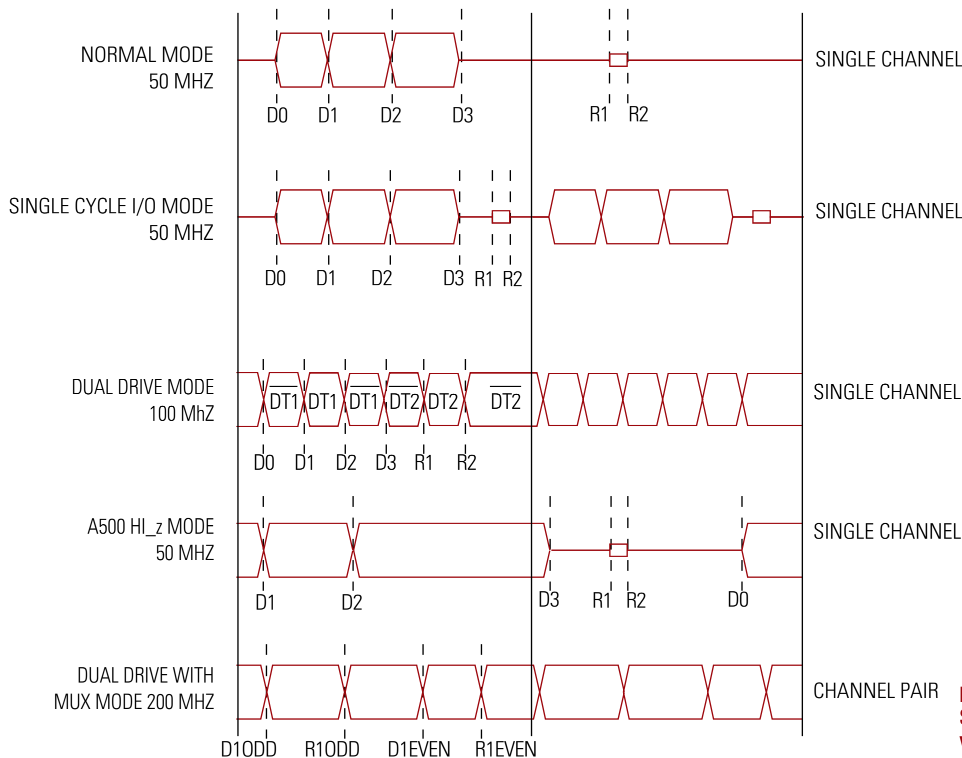


Figure 52
Six edges/pin can generate data in each 20 ns vector cycle.

words, either the drive or compare data can be first in the cycle. This order can also change on-the-fly, under control of the pattern, as long as timing conditions are not violated.

Another way to go beyond 50 MHz is to use a dual drive mode. In this mode, the drive and compare edges can drive two independently programmed data values to the device within a 50 MHz cycle. This means that 100 MHz data can be generated and formatted within the timing capabilities of the system without a trade-off in pin count or memory depth.

A third technique that surpasses 50 MHz uses the multiplex (MUX) mode. In MUX mode, two digital channels are combined at the formatter, not at the digital channel card or on the Device Interface Board. This technique generates up to 100 MHz of fully formatted I/O data. In this mode, the combined pattern data memory from the two channels provides up to two mega-vectors of depth. The channels are individually programmed for MUX mode operation, which, for example, allows one pin to operate at 100 MHz and the rest of the 190 system pins to operate at 50 MHz or less. The only MUX mode trade-off is reduced pin count. All formats, data, and memory depth are available.

A fourth method combines the dual drive and MUX modes. With this technique, 200 Mbit/second drive data rates are achievable. By programming the desired pin and its MUX'd pin in dual drive mode, the drive and compare edges from each pin combine to generate the 200 Mbit/second data stream. At 200 Mbit/second, the data uses non-return to zero (NRZ) formatting.

Two additional modes control the driver transitions to Hi-Z mode. A special mode called A500_hi_z, simulates the A500/A520/A540/A550 digital operation. There is also a Hi-Z mode that supports a return to Hi-Z format. In this mode, the pattern drives to the data value and returns to a Hi-Z state, which is sometimes required when testing bus interface device pins.

The A565 digital capability is a 25/50 MHz test system with a maximum base rate programmable to 25 MHz. It is capable of normal mode at 25 MHz, single cycle I/O mode at 25 MHz, and dual drive mode at 50 MHz.

Edge Agility

The A585/A575/A565 timing generators are available on a per pin basis. Each pin in the system can generate six independent edges, including:

- D1 and D2 - Drive edges
- D0 and D3 - Driver enable edges
- R1 and R2 - Receive window edges

The D1 and D2 edges generate the drive waveform shown in figure 52. The D1 edge designates the beginning of the edge, and the D2 edge defines the return edge. If the data is NRZ formatted, then only the D1 edge is used. If the format is return to zero (RZ), then the D2 edge returns the waveform to zero.

The D0 and the D3 edges enable and disable the driver respectively. The D0 edge designates when the driver comes out of a Hi-Z state and becomes active. The D3 edge designates when the driver goes into a Hi-Z state. These edges can be active within the drive cycle for normal A585/A575/A565 operation, or within a compare cycle to emulate the A500_ hi_z mode operation.

When generating a complement surround format on an I/O pin, D0 edge tells the driver when to complement the data before the data value. D1 tells the driver when to drive to the designated value. D2 determines when to return to complement, and D3 determines when to go to Hi-Z for a compare cycle. This combination of edges and complement surround verifies device operation under proper setup and hold timing parameters for both data and address pins.

The R1 and R2 edges strobe the comparator to determine if the data correctly compares with the data contained in pattern memory. (The edges can also strobe data into the digital signal capture memory.) The combination of R1 and R2 edges generate an active window strobe between the two edges. If a threshold is violated at anytime during the window, a failure is recorded. This allows the window strobe to capture device glitches.

All edges have ±350 ps of placement accuracy. This means that the maximum error between any two drive channels or any two comparator channels is ±350 ps. The error between any driver and any comparator is ±500 ps, which represents the overall accuracy of the system. This accuracy is specified at the device pin, so it includes the signal path on the DIB. Time Domain Reflectometry (TDR) calibrates all digital signal paths in the test head and DIB. All edges on the A565 have ±1 ns edge placement accuracy. (Refer to the System Configuration Section of the document for a summary of the differences among the A585/A575/A565 systems.)

Edge resolution is 1/64 of a TimeMaster clock cycle, or between 78 and 100 ps for programmable TimeMaster clock frequencies from 160-200 MHz. Deskew adjustment provides greater resolution, which is needed for edge search functions and for finer placement. Deskew adjust has a resolution 1/256 of the TimeMaster clock period, equivalent to 19 ps at 200 MHz.

Timing Sets and Edge Sets

The A585/A575/A565 systems have 1,023 timing sets, that allow on-the-fly time changes, a feature required by VLSI and mixed-signal devices. The test system uses a palette scheme for time set addressing. Each channel is backed by 32 edge sets. Each edge set contains six values, one for each edge per pin. The palette scheme increases the flexibility of these time set memory edge sets.

There are 1,023 locations of time set memory. Each location contains one unique edge set address for each of the test system's digital pins. See figure 53.

The A585/A575/A565 systems also provide edge masking. One edge set can be defined as a mask. Edge masking prevents the timing generator from creating an edge and also affects the data format within the cycle. The

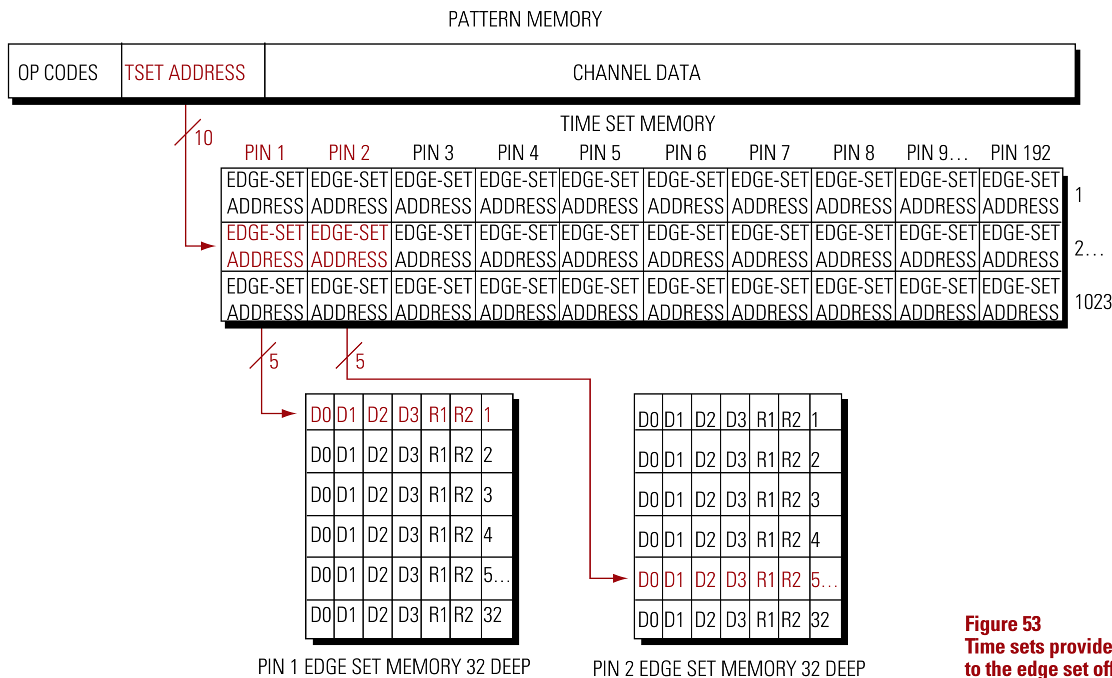


Figure 53
Time sets provide an indirect addressing capability to the edge set offering maximum flexibility.

receive window strobe is an example of edge masking. If the device has a pin that changes state and is expected to remain in that state for a large number of cycles, then the R1 edge can be used to open a compare window; the R2 edge can be masked so that the window will remain open for as many cycles as desired. In this instance, masking helps guarantee that when a device pin such as a status flag is enabled, it will remain enabled throughout the required set of vectors and will not glitch between states. See figure 54. The edge mask function requires only two edge sets, one to define the R1 and R2 edges, and one to mask the R2 edge.

Timing sets can change vector cycle time on-the-fly to verify on-board device memory where read/write cycle times may be different. The timing sets can also be used to change the divider value that generates the T0 and C0 clock rates at 50 MHz or 25 MHz on the A565.

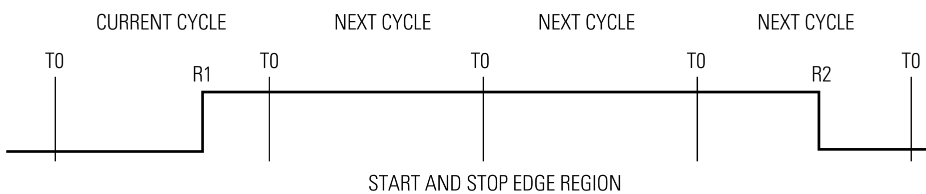


Figure 54
With edge masking, a compare window can be opened over multiple vector cycles.

Drive and Compare Formats

The A585/A575/A565 test systems provide 29 drive and compare formats that simplify the generation of different digital waveforms. See figure 55. Drive formats include:

- NRZ - Non return to zero and its complement
- RZ - Return to zero and its complement
- RO - Return to one and its complement
- CS - Complement surround and its complement
- CLKHI - Clock high in each vector
- CLKLO - Clock low in each vector
- OFF - Driver tristate
- FHI - Force driver to a static high
- FLO - Force driver to a static low
- DRVCLKHI - Clock high in drive cycles only
- DRVCLKLO - Clock low in drive cycles only
- DRVHI - Force a high in drive cycles only
- DRVLO - Force a low in drive cycles only

Compare formats include:

- CMPPAT - Compare to pattern data
- CMPHI - Compare to high in each vector
- CMPLO - Compare to low in each vector
- CMPMID - Compare to midband in each vector
- CMPLOG - Compare to logic in each vector
- CMPMASK - Mask compare results in each vector
- CMPOFF - Disable compare edges
- RCVHI - Compare high in receive cycles only
- RCVLO - Compare low in receive cycles only
- RCVMID - Compare midband in receive cycles only
- RCVLOG - Compare logic in receive cycles only
- RCVMASK - Mask compare results in receive cycles only

The static formats help simplify the process of debugging test programs.

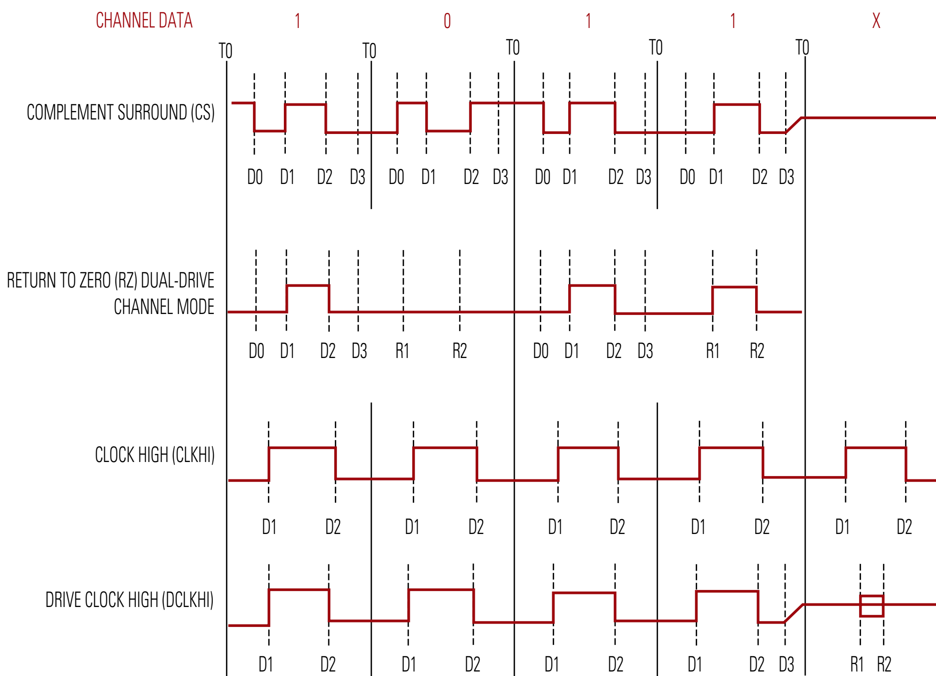


Figure 55
There are 29 drive and compare formats available on the A585 Advanced Mixed-Signal Test System.

HISTORY RAM FOR FAILURE ANALYSIS

For full debugging capability, the digital channels have a 4K deep history RAM that records failure information on each pin. The history RAM can operate in numerous modes and can capture both drive and receive data on all pins for all cycles. Using a pattern microcode to define the cycles, it can capture qualified cycles, which are predetermined by the user. It can also capture only failures. This function is 63 failures deep. The history RAM can begin capture on the Nth predetermined cycle. The captured data can be defined on a per pin basis as either pass/fail information or as logic data. Finally, this RAM also captures sequence control information such as cycle count, vector number, and flag status.

In each operating mode, a number of features can isolate any type of problem in any size pattern. Some of the features that provide this powerful debugging capability include:

- Global mask of compare for N cycles
- Capture until full
- Compress repeat cycles
- Halt after N cycles
- Halt on fail
- Inhibit halt on fails
- Inhibit halt on N cycles

DIGITAL CHANNEL CARD

The Digital Mainframe board and the digital channel card are the two key elements of the A585/A575/A565 digital channel. The digital channel card, which interfaces the device pin to the test system, includes the driver, a comparator, dynamic load, access to the dc matrix, access to Time Domain Reflectometer calibration, and a Per Pin Parametric Measurement Unit (PPMU). As shown in figure 56, each channel is programmable on a per pin basis.

The 50 Ohm driver provides three voltage ranges that cover -4.0 V to +7.0 V operation. The comparator has an operating range of -4.0 V to +7.0 V as well. The levels for V_{IH}, V_{IL}, V_{OH}, and V_{OL} can be programmed with 1 mV of resolution. The dynamic load provides an operating range of -4.0 V to + 7.0 V for the commutation point voltage (VCP) and can provide dynamic load currents up to 50 mA with 5 µA resolution. Similarly, the A565 voltage ranges cover -2.0 V to +7.0 V operation.

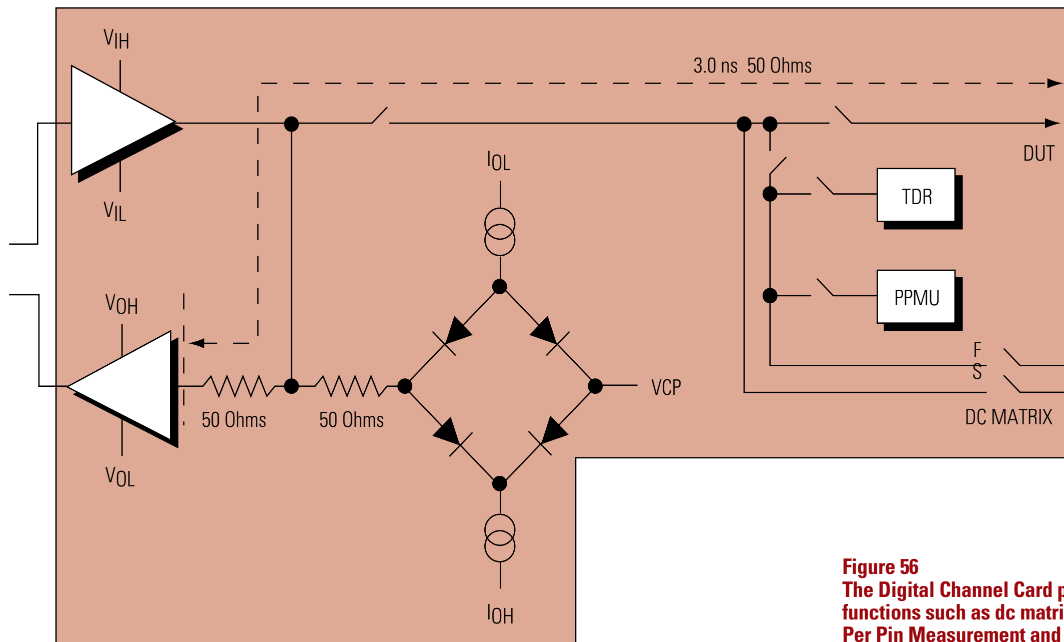


Figure 56
The Digital Channel Card provides access to all functions such as dc matrix, Time Measurement, Per Pin Measurement and TDR for calibration.

The dynamic load can act as a transmission line termination of 50 Ohms. This mode allows the A585/A575/A565 to terminate devices with I/O pins. An I/O pin can be terminated to a different voltage than one of the two driver levels. For example, a line could be terminated to 2.5 V to keep the load on a CMOS device output symmetrical. The driver levels could then be set to the correct V_{IH} and V_{IL} levels of 0 V and 5 V, respectively. (The A585/A575/A565 digital channel card also supports the traditional mode of operation, which terminates only output pins and uses the driver to force a low voltage.)

The load seen by the DUT is best modeled as a transmission line. All of the capacitance in the pin electronics and in the path to the device is distributed. A TDR of the path using a 1 ns rise time shows the lumped capacitance along the path is less than 2 pF. The device loading model that best represents the tester is a 50 Ohm transmission line that is 3 ns in length. To calculate the actual length, add the electrical length of the wiring on the DIB to the 3 ns path length from the Iso-Pins™ to the pin electronics. The electrical length of wiring on the DIB can be estimated at 1.77 ns/foot or 0.147 ns/inch. A typical 6 inch pc trace yields a total path length of 3.9 ns.

Every digital channel provides access to the Time Measurement Subsystem. This instrument can make single shot time measurements on single channel signals such as duty cycle, frequency, and rise/fall time. The Time Measurement Subsystem can also make measurements between digital channels and between analog to digital channels for propagation delay and skew.

Every digital channel also has access to the dc matrix, which allows the digital pin to use the standard V/I, the Analog Pin Unit (APU), the Advanced Analog Pin Unit (AAPU), the High Current Unit (HCU), and any other instrument connected to the dc matrix. The ability to access a wide variety of resources on a per pin basis is built into the digital channel card, simplifying the design of the Device Interface Board.

For continuity, leakage, and output voltage parametric measurements, the A585/A575/A565 has a four-quadrant parametric measurement IC on every digital pin. The Pin Parametric Measurement Unit (PPMU) can perform dc parametric measurements in parallel, while forcing voltage and measuring current, or while forcing current and measuring voltage. The PPMU operates over a -4 V to +7 V range in the A585/A575, -2.0 V to +7.0 V range for the A565, and offers current ranges from 200 nA to 2 mA. The settling time for measurement on all pins can be programmed to achieve the fastest possible parametric testing.

Opens and shorts testing is accomplished automatically using simple software commands that can execute a continuity test with only one statement.

140 MHZ HIGH-SPEED DIGITAL CHANNEL OPTION

As an option in the A585 and A575 models only, 140 MHz high speed digital channels can be substituted for the standard digital channels. The high speed option allows the use of return formats above 100 MHz and up to 140 MHz with improved pulse width specifications. Please refer to the specifications section later in this document.

SUPERCLOCK OPTION

In the A585 and A575 models, the Superclock provides a high speed clock signal with an operating fre-

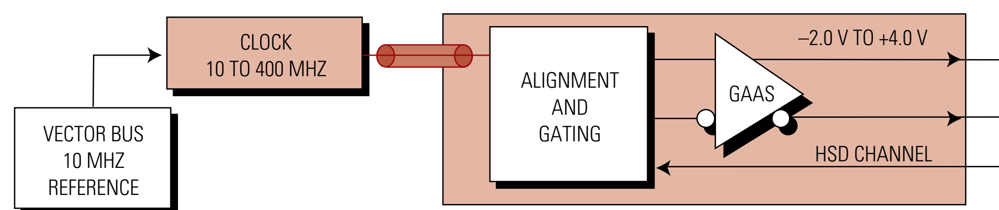


Figure 57
The Superclock option provides a synchronized 400 MHz clock source for high-speed device testing.

quency range of 10 to 400 MHz. The clock voltage swings are programmable over a 500 mV to 4.0 V range, with levels between -2.0 V to +5.0 V. The duty cycle is programmable over a 40% to 60% range. The drive only clock output can be used either single-ended or differentially. In a free-running mode, the clock signal is available asynchronously to the system clock T0. The Superclock signal can be gated ON/OFF by a dedicated digital channel, which will then synchronize the Superclock output with the system T0 clock. The Superclock option consists of a mainframe synthesizer and a test head channel card. Refer to figure 57.

SUPER SPEED SERIAL PIN

The maximum serial data rate with the standard digital channels is 200 MBits/second, when the dual drive, multiplexed mode is used, as described previously. To significantly increase the data rate in the A585 and A575 models to accommodate the demands of disk drive (PRML) and ATM devices, Teradyne has developed the Super Speed Serial Pin (SSSP). See figure 58. The SSSP replaces a standard digital channel card in the test head. The SSSP card provides a differential drive pin and differential receive pin, operating simultaneously at a maximum serial data rate of 400 Mbits/second. The drive pins have a 50 Ohm backmatched termination; the receive pins are terminated to a programmable voltage through 50 Ohms. Each wire of each differential pair has Per Pin Parametric Measurement Unit (PPMU) circuitry attached to it, so full parametric measurements can be made on the HI and LO drive and receive lines of each device pin as needed.

The SSSP can support ATM/Sonet 622 MBits/second data rates by multiplexing two SSSPs at the DIB. The SSSP can be used in conjunction with the Digital Signal I/O Memory, with data loaded directly into the Smem, rather than encoded into the pattern. Received data can be captured directly to the Digital Signal I/O dig_cap. The SSSP channel card has direct internal connections to the Superclock and the Time Jitter Measurement System. A maximum of 8 driver/receiver pin pairs at 400 Mbits/second data rate can be installed in the A585.

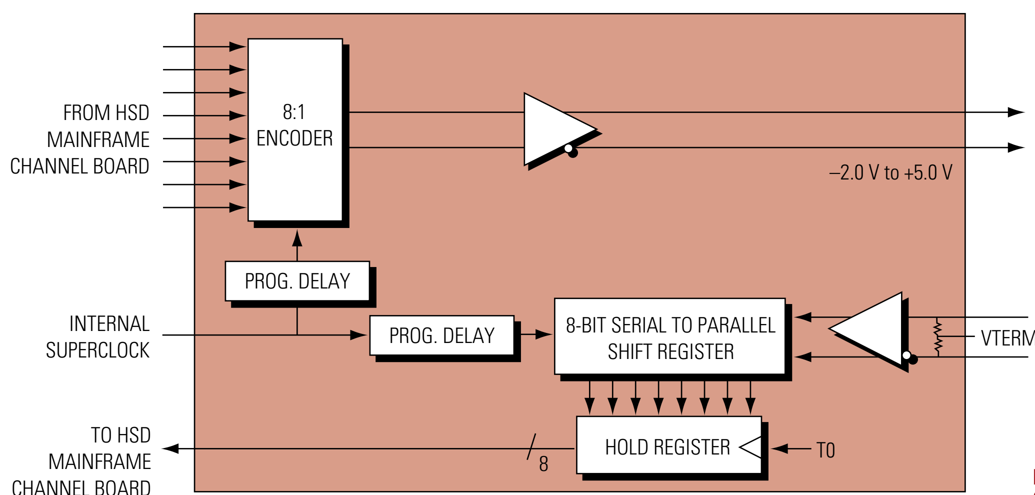


Figure 58
Super Speed Serial Pin Channel Card option

AC Instrumentation and Test Capabilities

Mixed-signal devices have multiple applications in automotive, television, telephone, computer, cellular telephone, and many other end products. Each of these applications interfaces to the analog world and each requires a unique type of analog signal to simulate the actual operating environment. These devices require mixed-signal test systems that can generate and measure signals ranging from high precision, ultra-low distortion for testing compact disk player devices, to ultra-high radio frequency for cellular applications.

Some of the A585/A575/A565 analog instrumentation that meets these diverse demands are shown in figure 59, including:

- Precision low frequency sources and digitizers, Very High Frequency (VHF) arbitrary waveform generators, and continuous waveform generators
- High frequency real time digitizers and high speed samplers
- Microwave waveform instruments

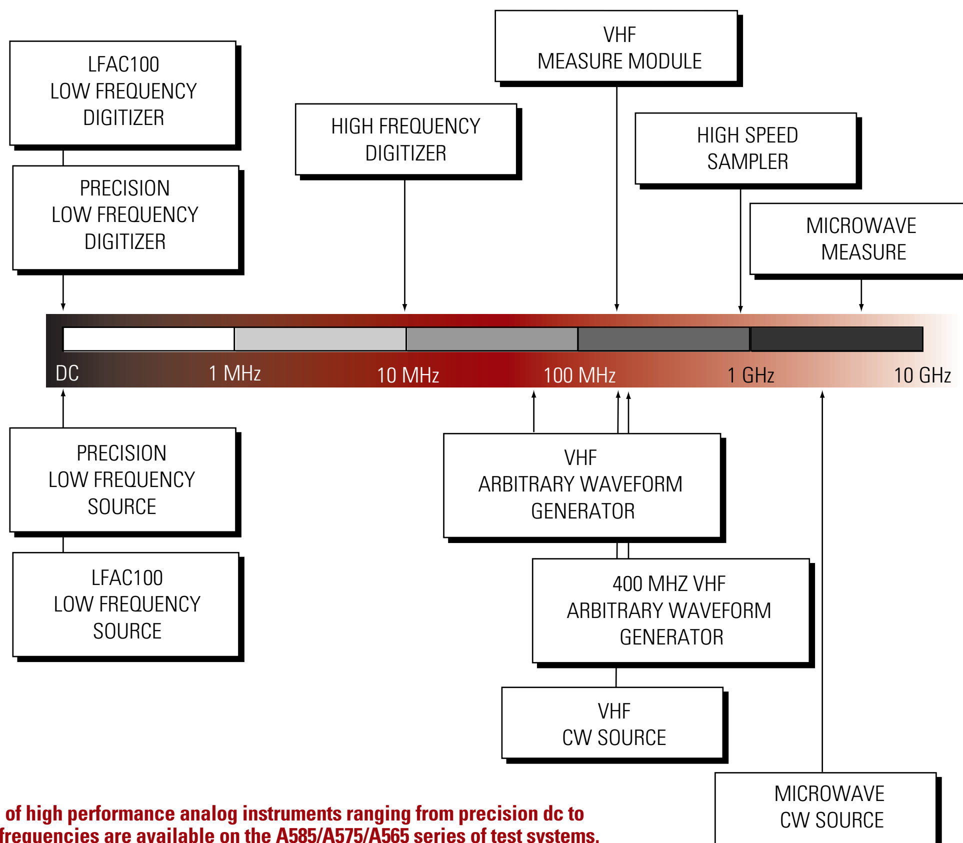


Figure 59
A full spectrum of high performance analog instruments ranging from precision dc to RF/microwave frequencies are available on the A585/A575/A565 series of test systems.

The Vector Bus III architecture ensures complete synchronization with digital patterns for these high performance analog instruments. The Vector Bus clocking architecture allows instruments to operate asynchronously with each other or relative to digital patterns, if desired.

ANALOG INSTRUMENT ARCHITECTURE

The analog instrument architecture is similar to the architecture of the A585/A575/A565 AVLSI digital pins. Each instrument consists of a source or capture memory with a controller, a formatter referred to as the conversion and filtering unit, and a test head channel card that provides a controlled impedance environment to the device as well as programmable control of signal levels between the device and tester. See figure 60. The source and capture memories are similar to the digital signal I/O memories. The

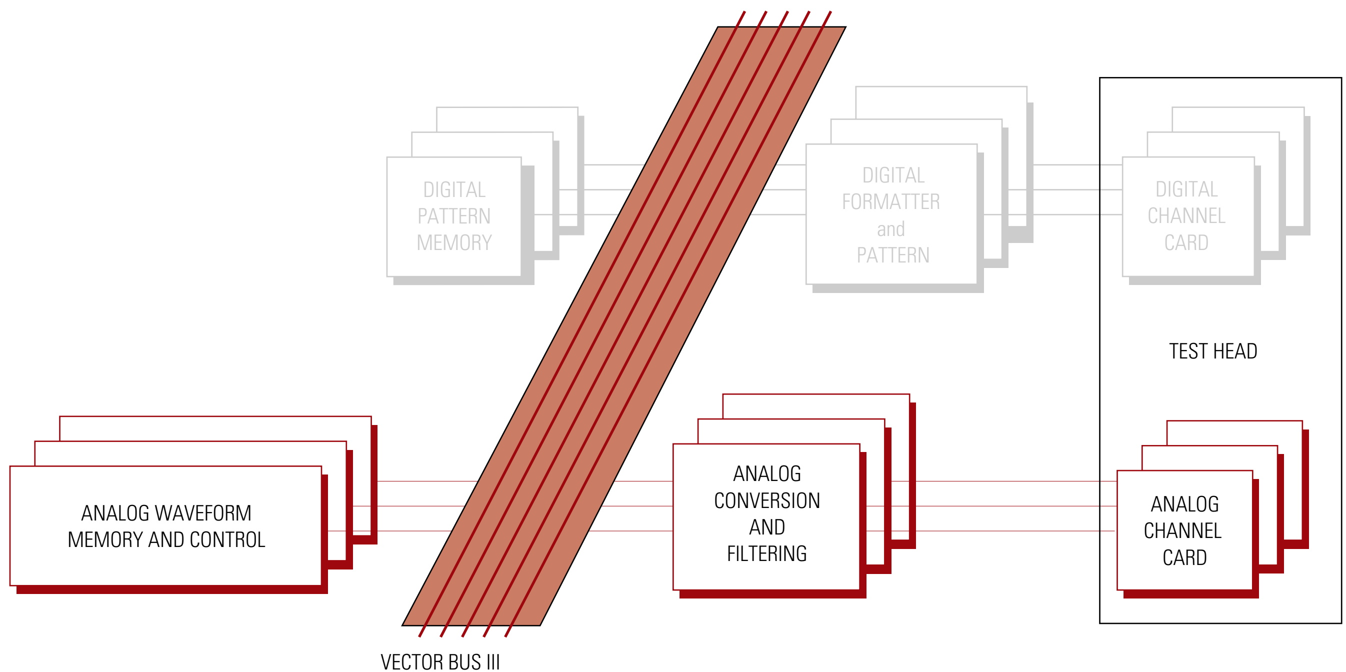


Figure 60
The architecture of the memory-based analog instruments is very similar to the VLSI architecture of the digital pins.

source memory (Smem) stores the waveform and waveform segments used for testing the device.

For testing video devices, the controller can create complex waveforms from simple segments for testing devices like those used in video applications. These complicated waveforms are nearly impossible to describe with a single mathematical function. However, when broken down into segments, they can be described with simple sine waves as shown in figure 61.

The data, which can originate in a file downloaded from the disk drive, is pre-calculated in the system computer or array processor and loaded into Smem. Smem clocks the data samples from its memory to the D/A converter in the instrument at the rate defined by the TimeMaster Analog (A0-A3) clocks. In addition, mixed-signal microcodes from the digital pattern memory control the instrument, allowing it to Vector-Lock to the digital pattern. This means a waveform does not have to begin with computer control. Instead, it can be triggered by the digital pattern so that every time the device program runs, the wave-

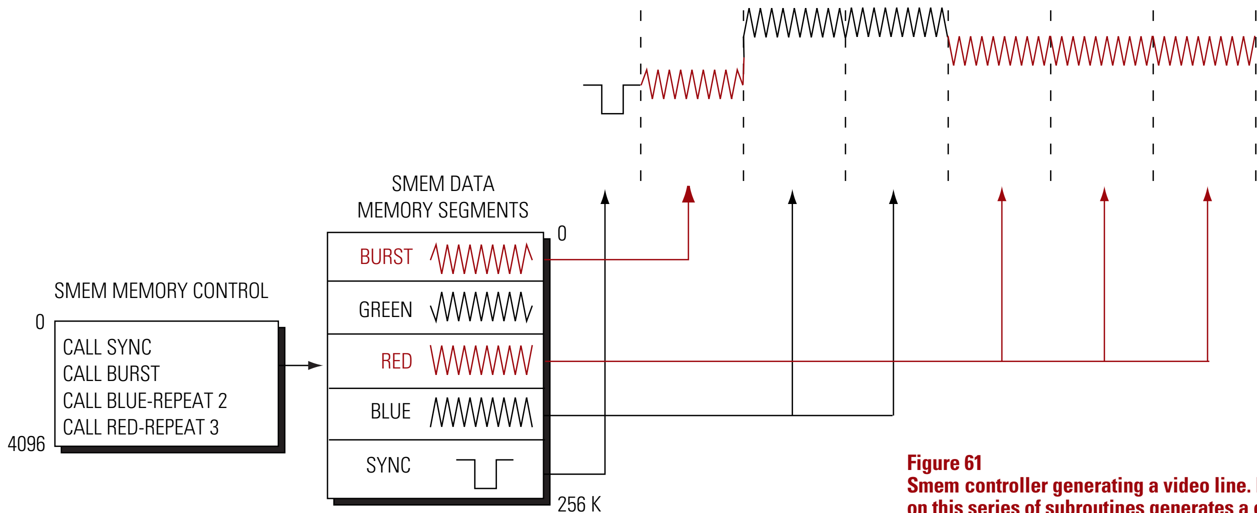
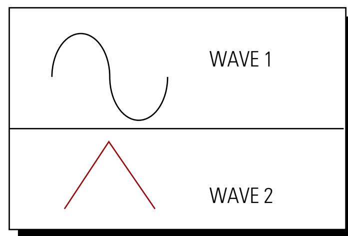


Figure 61
Smem controller generating a video line. Looping on this series of subroutines generates a complete video frame.

form starts at precisely the same clock cycle as the device. Some of the available microcodes are shown in figure 62, including:

- Start waveform and continue to run
- Start waveform and run once
- Start new waveform at the end of current waveform to provide phase continuous switching of signals
- Start new waveform at the end of the current waveform and execute once
- Go to the next waveform at the end of the current waveform
- Go to the next waveform and execute it once
- Stop immediately
- Stop at the end of the current waveform
- Trigger to start the digitizer capturing data
- Resync to allow the T0 digital clock and the analog clocks to align their edges for repeatable phase alignment

This level of control makes applications repeatable every time the program is run and provides reliable correlation from system to system. It also makes it easier to generate complex waveforms synchronously with digital patterns as required by ISDN, disk drive, and FAX modem devices.



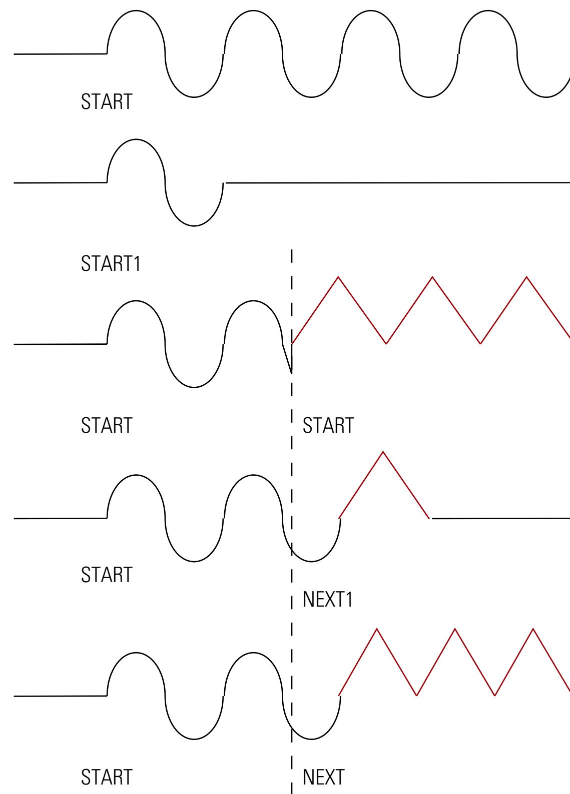


Figure 62
A variety of mixed-signal microcode commands control switching between waveforms. The action can be performed immediately or phase continuously.

ANALOG INSTRUMENTATION

Analog Instrument Channel Card

Every analog instrument channel card is custom designed for each instrument type. Precision Low Frequency Source, Precision Low Frequency Digitizer, Very High Frequency Arbitrary Waveform Generator, High Frequency Digitizer, and Microwave Continuous Wave Source channel cards are matched to the mainframe instrument. The channel cards used in source instruments provide impedance matching to the device, signal amplitude control, plus time measurement system and dc matrix access. The capture instrument channel cards provide selectable input impedances, voltage ranging (amplification), and access to the time measurement system and dc matrix. These functions provide a high performance level at the DUT and reduce the applications hardware required on the device interface board such as amplifiers, attenuators and relay matrixes are unnecessary, as shown in figure 63.

AC instrument channel cards can also access the Test Head Analog Distribution System (THADS) Bus. The THADS Bus allows an ac instrument to be rerouted to other device pins without using additional relays on the device interface board (DIB), giving true tester-per-pin capability for ac signals.

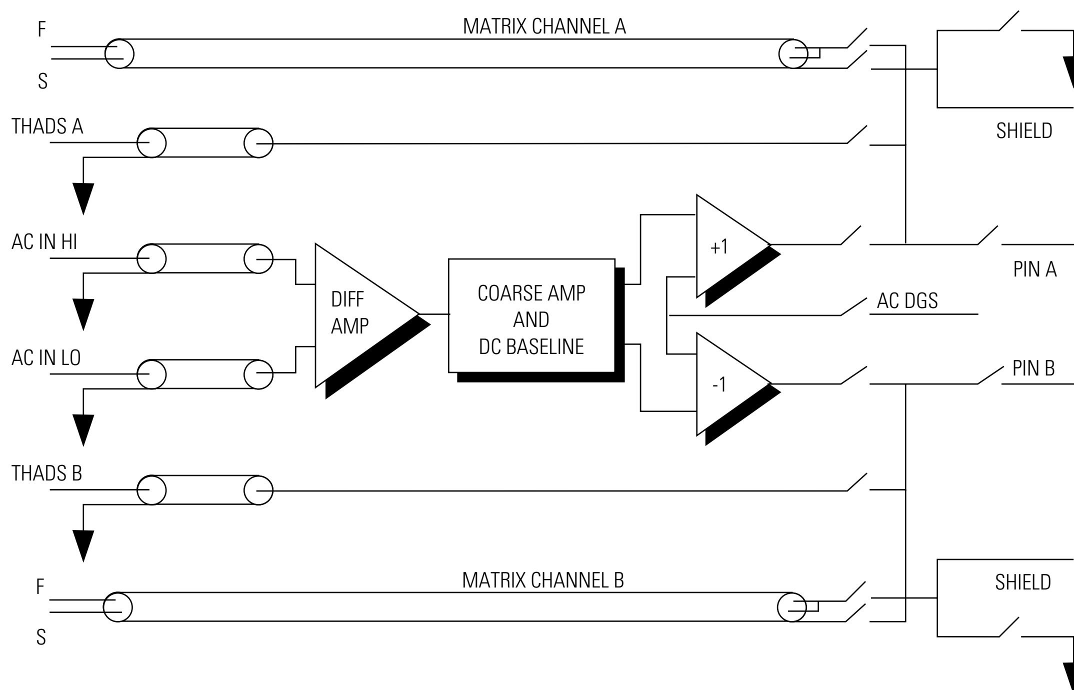


Figure 63
The Precision Low Frequency Source (PLFS) analog channel card provides access to time measurement functions, to an ac distribution bus in the test head (THADS) and to dc matrix functions.

Precision Low Frequency Source

The Precision Low Frequency Source (PLFS) is a memory-based instrument designed for applications requiring ultra-low distortion performance in an operating bandwidth of up to 500 kHz. See figure 64. It is used to test precision converters, telecommunications and audio devices.

The PLFS is based on a proprietary sigma-delta 20-bit architecture. The memory is 64 K deep by 20-bits with a local 512 waveform segment controller. There is also an optional 1 Meg by 20-bit memory with the same waveform controller. Waveforms can be differential or single-ended at ±11.0 V_{PK}. A selectable output impedance of 25 Ohms or < 1 Ohm allows the instrument to match a variety of applications and minimize error sources. To provide optimum dynamic range, dc offset is programmed with a dc baseline generator on the channel card added to the signal in the PLFS channel card. The PLF Source can generate a 1 kHz sine wave at better than -115 dB total harmonic distortion (THD) and better than -110 dB of total signal-to-noise over a 20 kHz range.

The PLFS contains a real time digital integrator that can generate ramp and triangle waveforms to better than 2 ppm linearity for testing precision converter devices and complex system silicon containing A/D converters. It also contains built-in linearity calibration correction that is applied to every sample sent to the D/A converter. Fine amplitude adjustment in the digital domain helps reduce the amount of analog signal processing in the signal path and provides an ultra-low-noise signal to the DUT. The PLFS can also access the Universal Bus architecture.

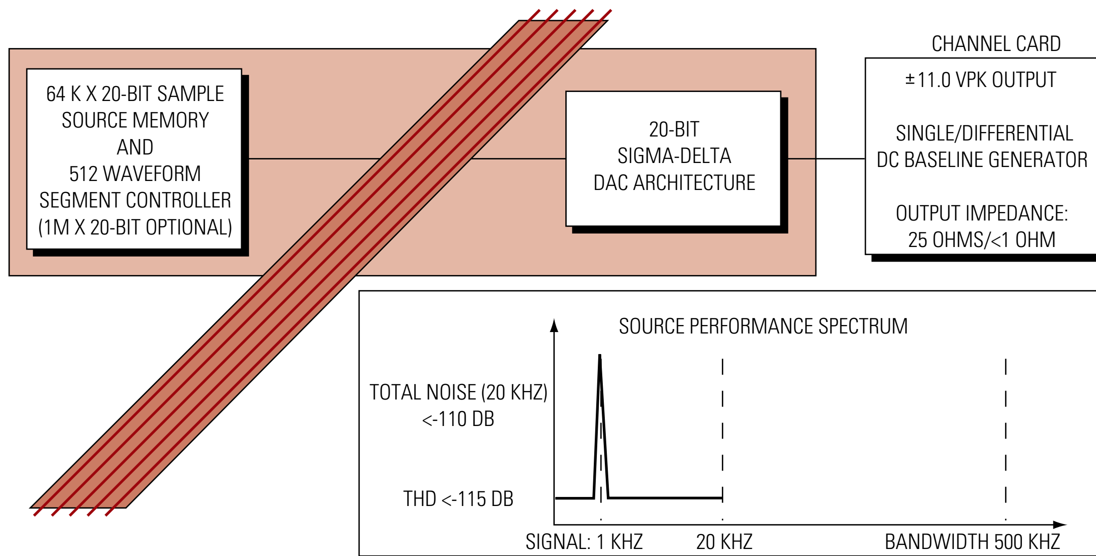


Figure 64
The Precision Low Frequency Source provides ultra-low distortion performance for testing mixed-signal devices.

Precision Low Frequency Digitizer

Audio, telecommunications, precision DACs, and data communications devices require very low distortion measurements. The Precision Low Frequency Digitizer (PLFD) with its 23-bit sigma-delta architecture was designed for these and other applications. See figure 65. The PLFD can make 1 kHz signal measurements with better than -110 dB of total harmonic distortion and better than -95 dB signal to noise over a 20 kHz bandwidth.

The total bandwidth of the instrument is 500 kHz. The capture memory is 256 K samples deep.

The PLFD channel card is very similar to the PLFS channel card. The dc offset generation capability removes dc components from the signal before gain is applied to maximize ac dynamic range. The PLFD can operate single-ended or differentially and can handle up to ±11.0 V_{PK} input signals.

The PLFD also provides programmable real-time digital filters that are time or frequency domain optimized. Depending on the type of measurement, it may be necessary to use a time domain based filter with low ringing characteristics to analyze an ISDN waveform against a pulse shape template. A frequency domain filter analyzes frequency response with very low ripple response in the passband. The PLFD also interfaces to the Universal Bus architecture.

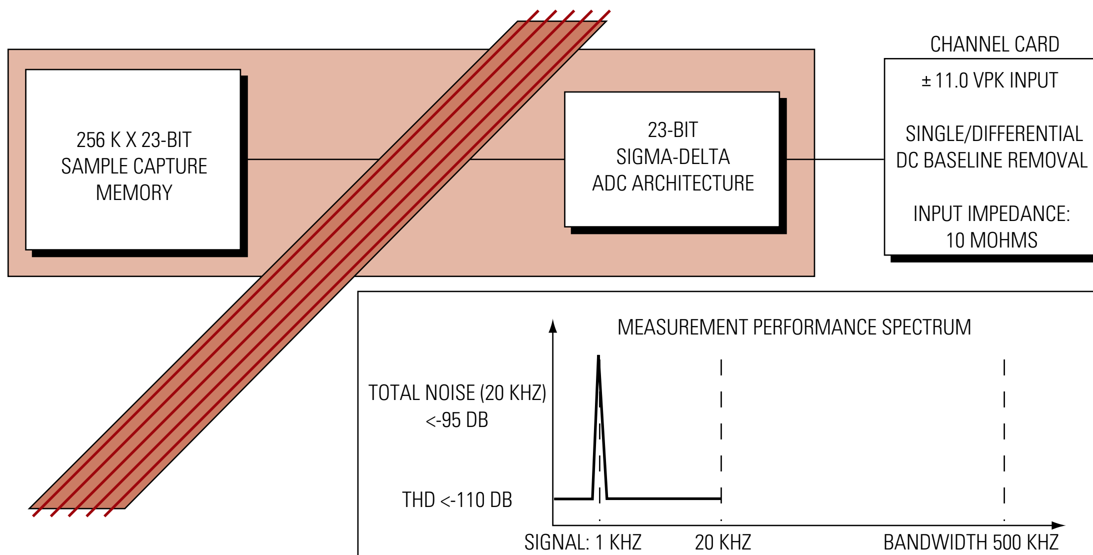


Figure 65
The Precision Low Frequency Digitizer includes sample memory, Vector Bus and conversion on a single board.

LFAC100

The Low Frequency AC Source and Digitizer (LFAC100) are memory-based instruments designed for applications requiring low distortion performance in an operating bandwidth of up to 100 kHz, such as telecommunications, audio and automotive. They feature high-level, simplified programming.

LFAC100 Source (Low Frequency AC Source)

The Low Frequency AC Source combines the features of function generator programming and arbitrary waveform generator in one module. Functions that can be programmed include ramps with control of rate and end points or period and amplitude of sawtooth; square wave with control of duty cycle and amplitude; sine wave with frequency, amplitude and phase control; and multitone with control of frequency components and amplitude. The arbitrary waveform function provide controls for what data array is input, number of samples, sample rate, maximum amplitude, and programmable filters. The arbitrary waveform generator has a 16-bit resolution. The

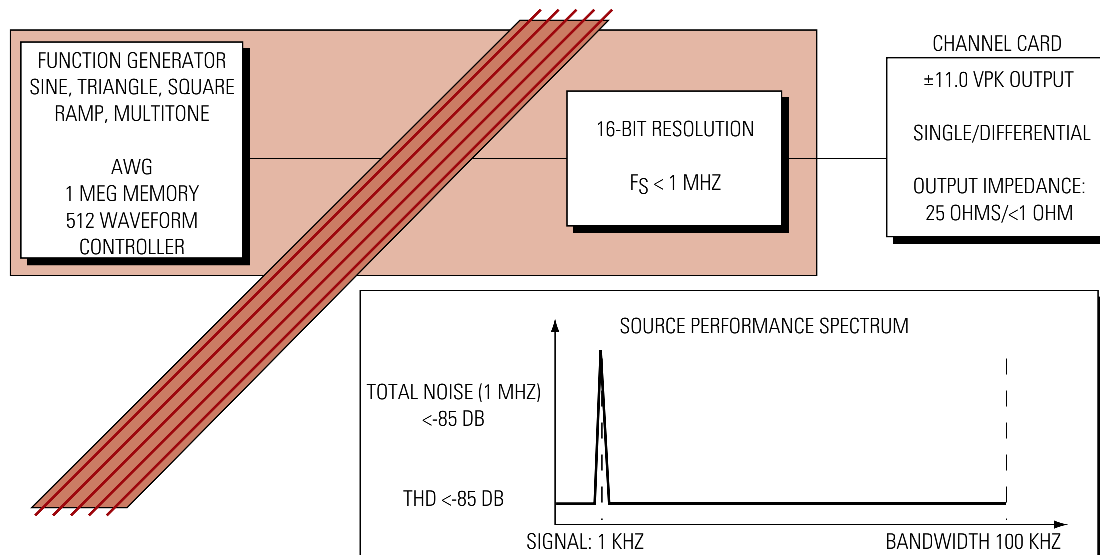


Figure 66
The Low Frequency AC Source

Low Frequency AC Source provides ±11.0 V_{PK} output with ±11.0 V dc offset, better than -85 dB performance, and a 100 kHz bandwidth. The output of the source can be either single-ended or differential, with a selectable output impedance. See figure 66.

LFAC100 Digitizer (Low Frequency AC Digitizer)

The Low Frequency AC Digitizer features 16-bit resolution and 100 kHz bandwidth. The input to the digitizer accepts differential inputs up to ±11.0 V_{PK} and provides ±11.0 V_{PK} of dc baseline removal. It has a 256 K sample capture memory depth. See figure 67.

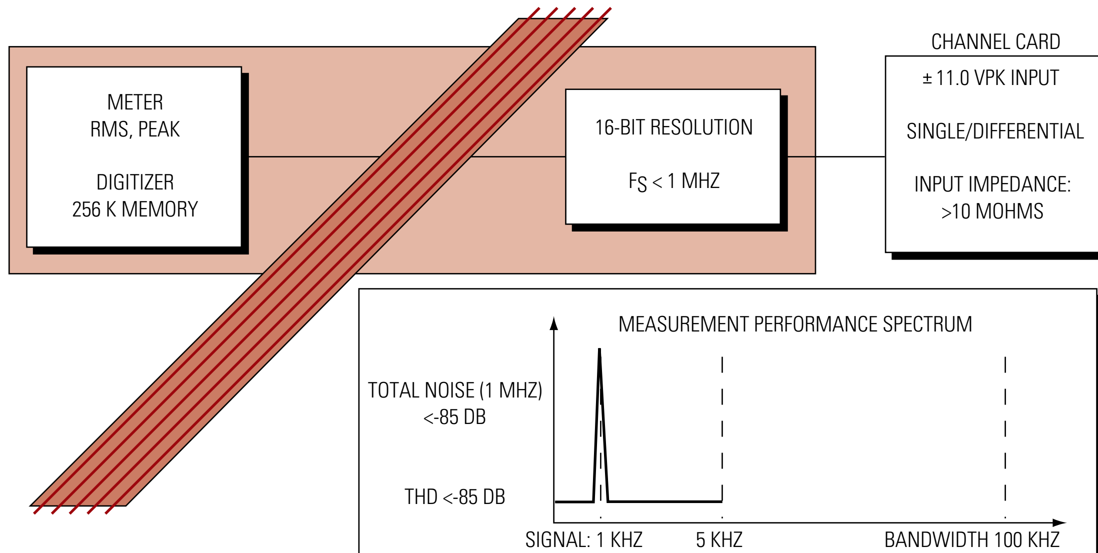


Figure 67
The Low Frequency AC Digitizer

Very High Frequency Arbitrary Waveform Generator

The Very High Frequency Arbitrary Waveform Generator (VHFAWG) shown in figure 68 contains a 256 K by 12-bit source memory or, optionally, a 1 M by 12-bit source memory, with a controller that can handle 4,096 waveform segments. An internal GaAs-based DAC provides 12-bit waveform resolution at up to 200 MHz sample rates. The bandwidth for arbitrary waveform generation is 80 MHz, which is necessary for testing current and future disk drive, Ethernet, and video devices. The instrument can also operate in a continuous waveform generation mode up to 200 MHz by generating sine waves that can be directly used for bandwidth measurements.

Inside the VHFAWG, a 4x clock multiplier and integer divider generates the appropriate sampling clocks based on the TimeMaster clock input. This allows for maximum flexibility on the TimeMaster Clock programmability.

The channel card provides amplitude control of ±2 V and the ability to add up to ±2 V of dc offset, assuming a 50 Ohm load. Level compensation to the DUT provides better than ±0.25 dB amplitude accuracy. If the device load is not equivalent to 50 Ohms, a simple command defines the load equivalent, and software makes the necessary adjustments to achieve the desired level at the DUT.

The instrument filters provide excellent step response characteristics for obtaining the clean and precise waveforms required for applications with demanding time domain characteristics such as video, Ethernet and disk drives. For example, the 80 MHz filter has a rise time specification of <8 ns and <8% over/undershoot characteristics.

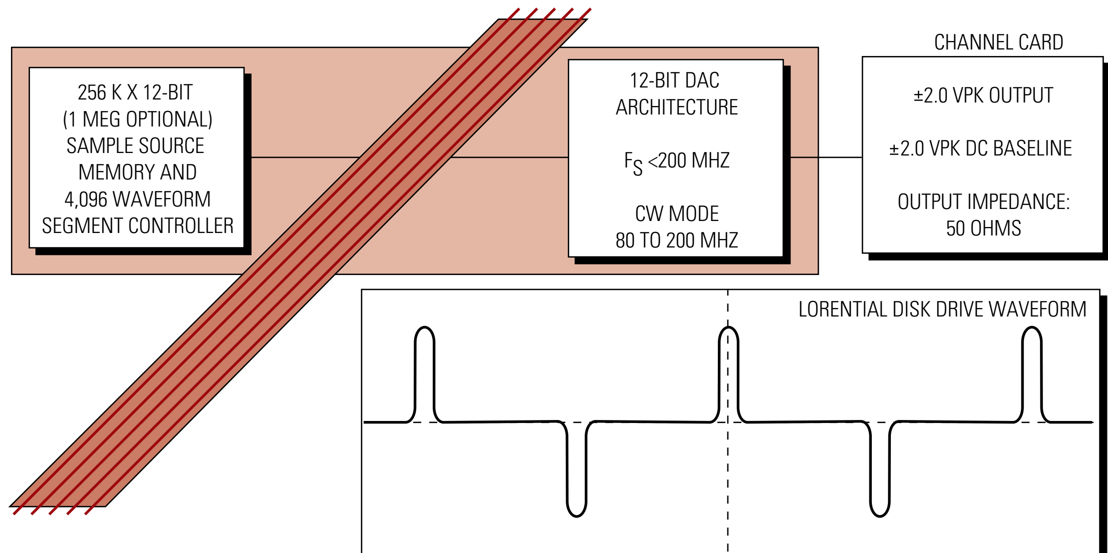


Figure 68
The Very High Frequency Arbitrary Waveform Generator produces signals for disk drive testing. The VHFAWG400 provides sample rates up to 400 MHz.

VHFAWG400

A 400 MHz version of the VHFAWG, called the VHFAWG400 is also available. The VHFAWG400 has a maximum sample rate of 400 MHz and an output bandwidth of 160 MHz for testing ATM and disk drive devices.

High Frequency Digitizer

The High Frequency Digitizer (HFD) illustrated in figure 69 is a 12-bit instrument that samples waveforms in real-time at up to 20 MHz sample rates. It has a 1 Meg sample memory 20 bits wide and can digitize signals over a ±20 V range with ±12 V of dc baseline removal. A 1 MHz signal can be digitized with less than -60 dB harmonic distortion and less than -77 dB noise.

Numerous low pass filters for antialiasing in the HFD include a phase linear 6.1 MHz filter required for testing video devices. A 256 kHz high pass filter allows analysis of distortion components in signals less than 128 kHz through a technique referred to as filter/amplify/digitize. This technique allows an additional 20 dB of dynamic range improvement. The HFD can also interface to the Universal Bus architecture.

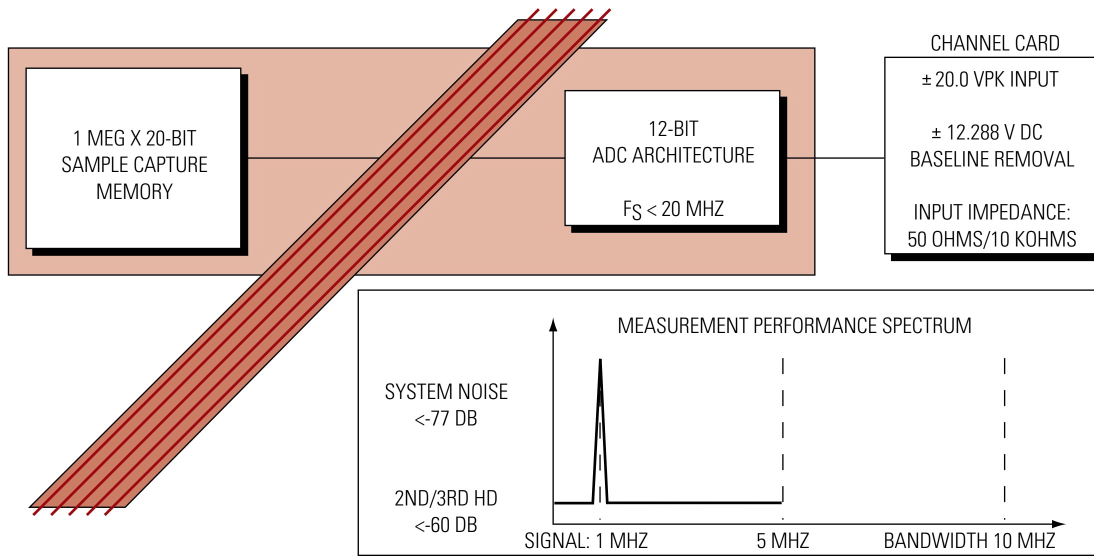


Figure 69
The High Frequency Digitizer analyzes performance of devices such as video, disk drive, and ISDN components.

Very High Frequency Continuous Waveform Source

For linearity tests on high frequency devices such as flash converters, it is necessary to generate very linear, low harmonic distortion sinewaves. See figure 70. The Very High Frequency Continuous Waveform Source (VHFCW) generates signals from 1 MHz to 250 MHz with 1 Hz resolution. These signals are generated with less than -70 dBc harmonic distortion.

The channel card provides amplitude control of ±2 V and the ability to add up to ±2 V of dc offset, assuming a 50 Ohm load. Level compensation to the DUT provides better than ±0.25 dB amplitude accuracy. If the device load is not equivalent to 50 Ohms, a simple command defines the load equivalent, and software makes the adjustments necessary to achieve the desired level at the DUT.

The VHFCW Source has a programmable frequency synthesizer with excellent frequency accuracy and resolution that derives its reference for synthesizing waveforms directly from the Vector Bus III so it is always synchronized to the entire test system.

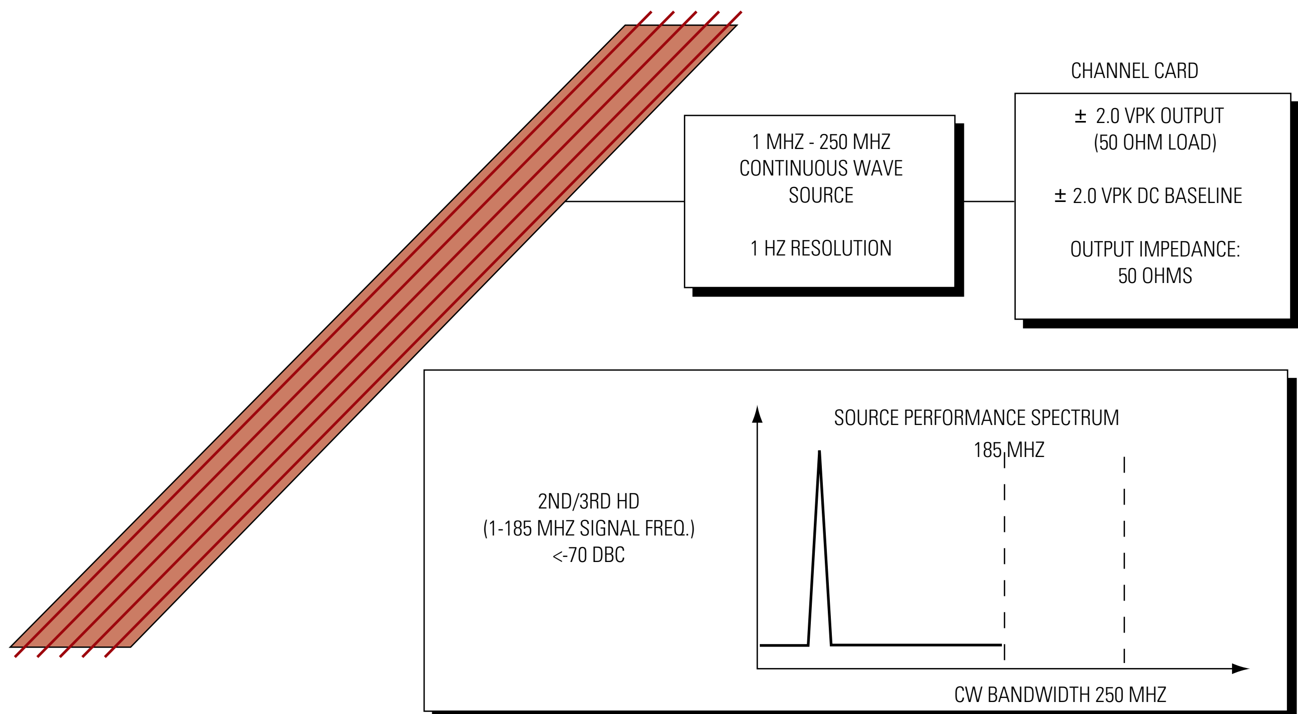


Figure 70
The VHFCW Source is an excellent input source for measuring linearity performance of flash ADCs.

High Speed Sampler (HSS)

The High Speed Sampler provides an under-sampling capability that handles applications requiring the capture of very high frequency waveforms and pulses such as those generated by palette DACs, disk drive, and Ethernet devices.

The HSS has a 256 K by 16-bit capture memory, a sampling head, and a channel card with a Successive Approximation Register (SAR) based reference DAC and timing control for sampling. The sampling head has selectable input impedance of 37.5, 50, 75, and 10 kOhms. The sampler head can be located on a channel card or on the DIB. The close location of the sampler head on the DIB to the device under test, eliminates frequency domain calibration because transmission line loss is not an issue and impedance can be appropriately matched. This location also provides significant noise reduction, so averaging of multiple acquisitions is unnecessary, directly impacting test time. The sampler has less than 100 µVrms of noise over the entire 1 GHz bandwidth, which translates to 11 nV/rt Hz.

The HSS provides a 1 GHz input bandwidth and can capture signals with an effective sampling rate of up to 100 GHz as shown in figure 71. The instrument resolution is programmable between 2- and 16-bits, with the Successive Approximation Register (SAR) architecture. The ability to adjust resolution ultimately affects overall timing since reduced resolution equates to reduced test time. Lower resolution conversions can be used for faster test speed when high accuracy is not required.

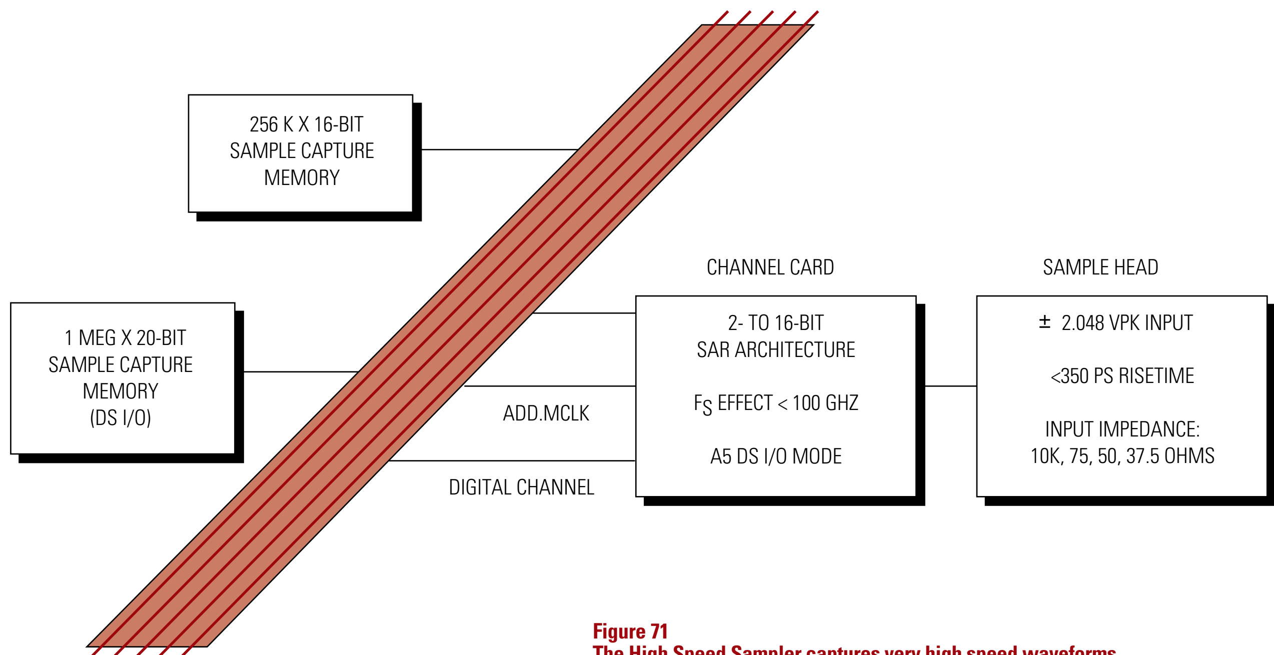


Figure 71
The High Speed Sampler captures very high speed waveforms.

Very High Frequency Measure Module

The Very High Frequency Measure Module extends the measurement capability of the A585/A575/A565 series of test systems to 250 MHz. It does this in two ways. The VHFMM contains a down conversion module that converts signals from 250 MHz down to a 1 MHz bandwidth. The instrument has its own programmable Local Oscillator with 1 Hz programmable resolution. The VHFMM also contains a sampler head that can be used to undersample signals up to 250 MHz. The VHFMM is extensively used in disk drive applications for making all types of analog measurements including frequency response and harmonic measurements. See figure 72.

TIME AND JITTER MEASUREMENTS

Of major importance in most modern device testing is the ability to measure the elapsed time between two events and the variation in timing of the edges of an event. Whether the two events are DUT generated or one is generated by the DUT in response to a stimulus from the test system, the measurement of the time between the two events must be measured precisely. Unlike other test systems which must measure time by using digital edge search techniques that are difficult to implement and consume test time, Teradyne's A585/A575/A565 test systems have precision instruments that measure the time between two events directly, using the signals themselves to control the time measurement. Variations between a reference edge and a DUT edge can also be measured directly. Both of these time measurement capabilities dramatically increase test system throughput and accuracy.

Advanced Time Measurement Subsystem

Every device pin has access to the A585/A575/A565 Advanced Time Measurement Subsystem (ATMS). The unique, multiple patented ATMS design provides a limitless measurement range. The instrument can access every device pin under program control through the digital, dc and analog channels to

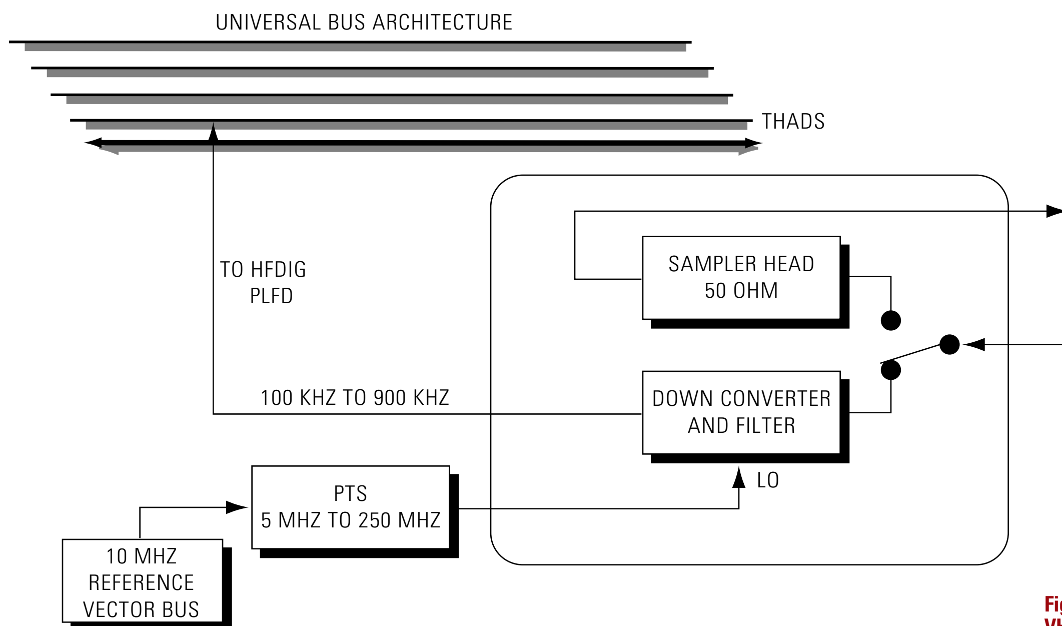


Figure 72
VHF Measure Module

make propagation delay, skew, frequency, rise/fall time, and other measurements. It is highly accurate with less than 1 ns error, and provides a flexible timer enabling system with the following features:

- Precounter/timer – selects a single event to start a measurement from a series of possible events
- Postcounter/timer – selects a single event to stop a measurement from a series of possible events
- Stop after start interlock – to force positive time measurements

When measuring skew between two pins, the stop after start interlock can be disabled so either pin can act as the start signal.

The ATMS has two primary modes: time and event. In time mode, the ATMS makes frequency, period, duty cycle, rise time, pulse width, and propagation delay measurements. In event mode, the ATMS counts the number of occurring voltage events and provides total counts or ratios of counted events to number of start events. The ATMS can make multiple successive measurements with its local 1 K measurement memory and can automatically perform averaging functions.

Time Jitter Digitizer

The Time Jitter Digitizer (TJD) provides the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems with the ability to precisely capture the time at which two user-specified events occur. The two events (A and B events in figure 73) can be specified based on device signal voltage level (threshold) and direction (slope). The TJD time-stamps each event or "writes down" the time at which each of the events occurs, within its capture rate ability. The TJD looks like a 16-bit counter running at 128 GHz, due to interpolation. The TJD has a better than 10 ps resolution. The TJD's capabilities are ideally suited to disk-drive and ATM clock and data jitter testing because the clock rates are fast and data patterns are known in advance.

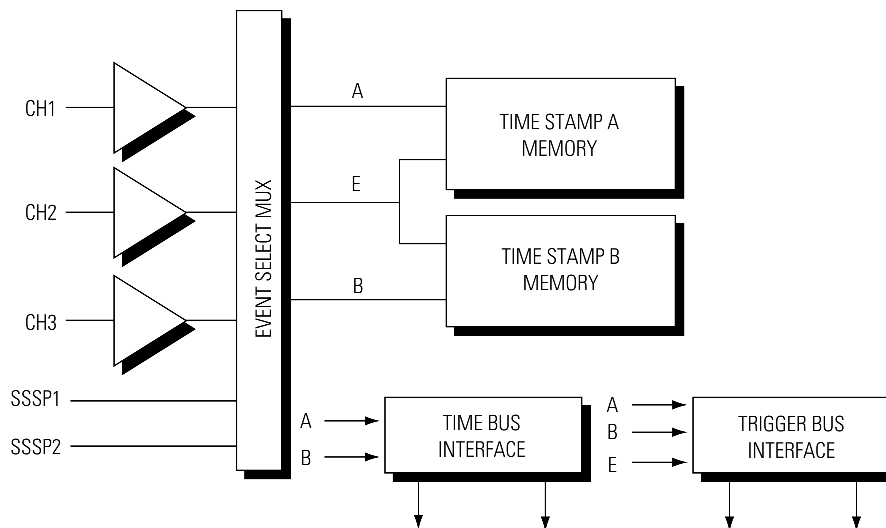


Figure 73
The Time Jitter Digitizer measures elapsed time between two events for direct measurement of phase, duty cycle or edge jitter.

The A and B event inputs can come from the same channel, as in a pulsewidth or period jitter measurement, or they can be from two different channels as in a phase jitter measurement. The TJD can capture successive events up to 28 MHz for each time stamper into a 16 K memory. Therefore, the two time stampers can be interleaved for 56 MHz operation. A third, enable, channel is provided to enable the time-stamping of either the A or B event. The TJD can also make frequency measurements greater than 350 MHz.

Figure 74 shows a simple example of an application for the TJD, where the width of a pulse is being measured. In this example, two events have been defined. Channel 1, rising through 1 V is defined as the A event, and channel 1 falling through 1 V is the B event.

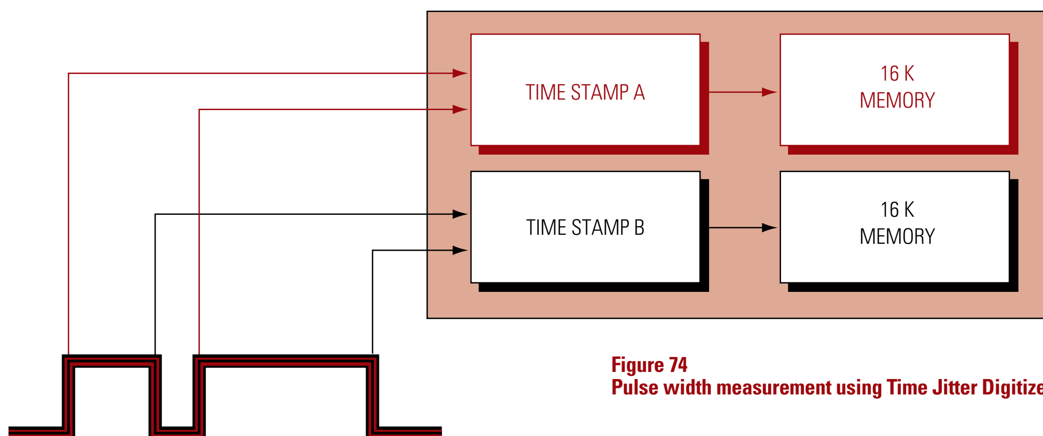


Figure 74
Pulse width measurement using Time Jitter Digitizer

MICROWAVE INSTRUMENTS

This section provides an overview of the hardware and software modules that are used in Teradyne's mixed-signal microwave test capability. Microwave capability is added to the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems by the addition of "front-end" modules that extend operating frequencies to the microwave region. These front-end modules up-convert signals from the ac sources, or down-convert signals from the DUT to drive the digitizers and measurement instruments described above. Refer to figure 75 for an interconnection diagram of the microwave front-end modules. For more details on Teradyne's microwave mixed-signal test capabilities, refer to the Teradyne document "A Blueprint for Mixed-Signal Microwave Test" (document number 05983A-0795).

Microwave CW Source

The Microwave CW Source consists of a Teradyne-designed, two-card set, one that plugs into the main-frame card cage of the test system and a companion channel card that plugs into the test head. It is an extremely fast and clean microwave source. This module is completely microwave-tight. It operates over a 4.5 MHz to 4 GHz range.

IF Modulation Source

The IF Modulation Source extends the frequency range of the VHFAWG to accommodate microwave devices by the addition of a frequency translation card set. The card set extends the frequency range to 5-180 MHz IF. The final output waveform is a product of the VHFAWG translated in frequency to a higher spectrum. The new frequency range signals are fully synchronized with ac measurements, other ac sources and digitizer modules.

Microwave Measure Module

The extension of the input frequency range of the measurement instruments to accommodate microwave devices is achieved by the Microwave Measure Module. The Microwave Measure Module accepts signals from 10 MHz to 6 GHz, over a +13 to -100 dBm dynamic range, and provides an IF output to feed either the High-Frequency or Precision Low-Frequency Digitizers. Up to 30 MHz information bandwidth is supported by the Microwave Measure Module for testing AM, FM, FSK, PSK, QPSK, π/4DQPSK, GMSK and I/Q demodulation modes.

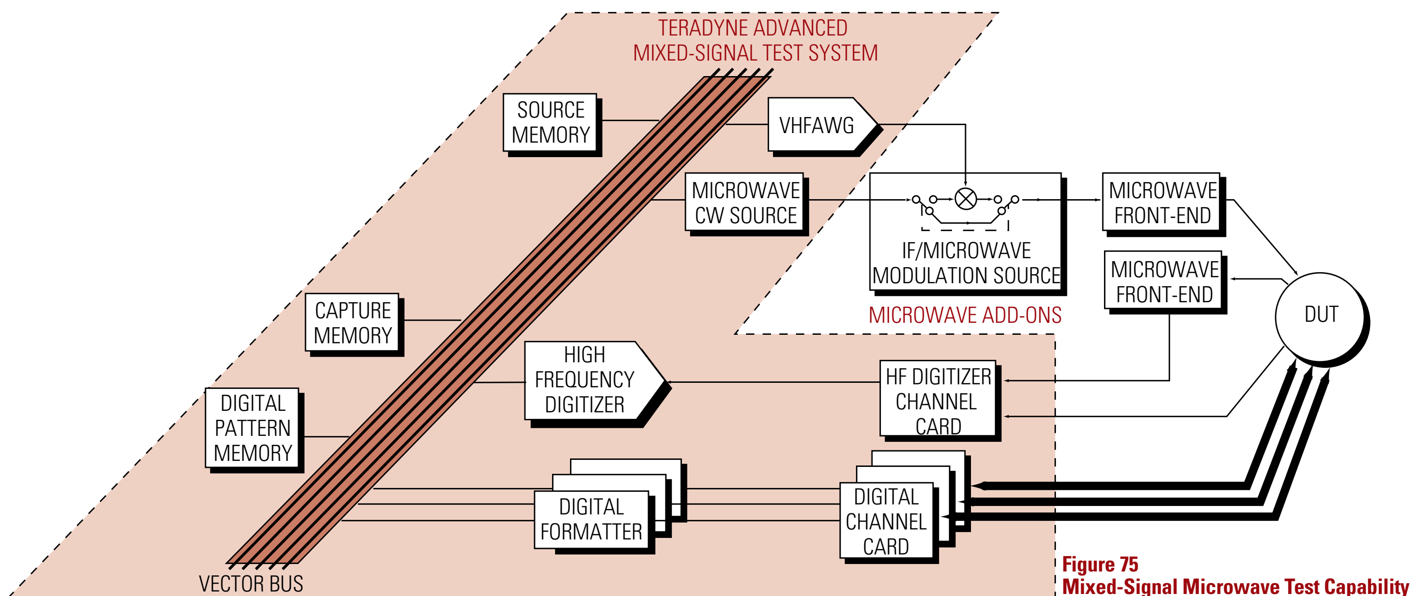


Figure 75
Mixed-Signal Microwave Test Capability

Microwave Vector Network Analyzer Module

The Microwave Vector Network Analyzer Module provides the built-in capability to extend automatic level and network calibration right to the pins of the DUT. It incorporates the functions of routing sources to and measurements from each of four pins, through two ports, minimizing or eliminating applications circuitry on the DIB. The Microwave VNA Module provides vector network measurement (S-parameter) capability and provides accurate calibration of load and reflection errors caused by the interconnects between the test system and the DUT.

The Microwave VNA Module moves the multiplexing and routing of signals from the DIB where it can pose many calibration problems, to the test head, where these problems are eliminated by making them part of the calibration path. The input section supports and routes two microwave or modulated sources to other sections of the module and, ultimately, to the DUT pins. Also, the module extends the source range by an additional -64 dBm to -114 dBm. A summing node within this section of the module provides Intermod test signals without DIB-based components, again simplifying calibration and DIB design. Internal calibration standards for open, short, load, and through termination are included within the module and are traceable to NIST standards. External calibration standards from the DIB out through the handler contactor or probe needles is fully supported. The dc matrix can also be accessed from the module.

Teradyne's Microwave Software Library

The extensive device test application library is continuously expanding to include new devices. Existing test routines include a variety of modulation techniques including AM, FM, FSK, PSK, QPSK, π/4DQPSK, GMSK and I/Q and standard tests such as S-Parameters, Third Order Intercept, Noise Figure, Isolation, Phase Noise, and Error Vector Magnitude.

DC Instrumentation and Test Capabilities

The dc instrumentation and test capabilities consist of the dc crosspoint matrix and the dc instruments described below.

DC CROSSPOINT MATRIX

The DC Crosspoint Matrix delivers dc signals from a series of instruments in the mainframe cabinet to multiple device pins. The digital and analog channel cards in the test head also have direct access to the dc matrix.

Figure 76 shows the 8 line by 48 pin fully guarded Kelvin (DC Crosspoint) matrix. Each pin includes a force and a sense pin and pins can have their guards grounded for applications that require low noise and minimum crosstalk. If the guard is driven, then overall system leakage in the signal paths can be reduced. The instruments connected to matrix lines can be disconnected, allowing the matrix to serve as a signal bus between multiple DUT pins. In addition, each matrix pin can have a dedicated Analog Pin Unit behind it.

DC SUBSYSTEM

Standard V/I Sources

On the A585, up to five dc sources operating at 60 volts and 200 mA can be connected to the matrix. These

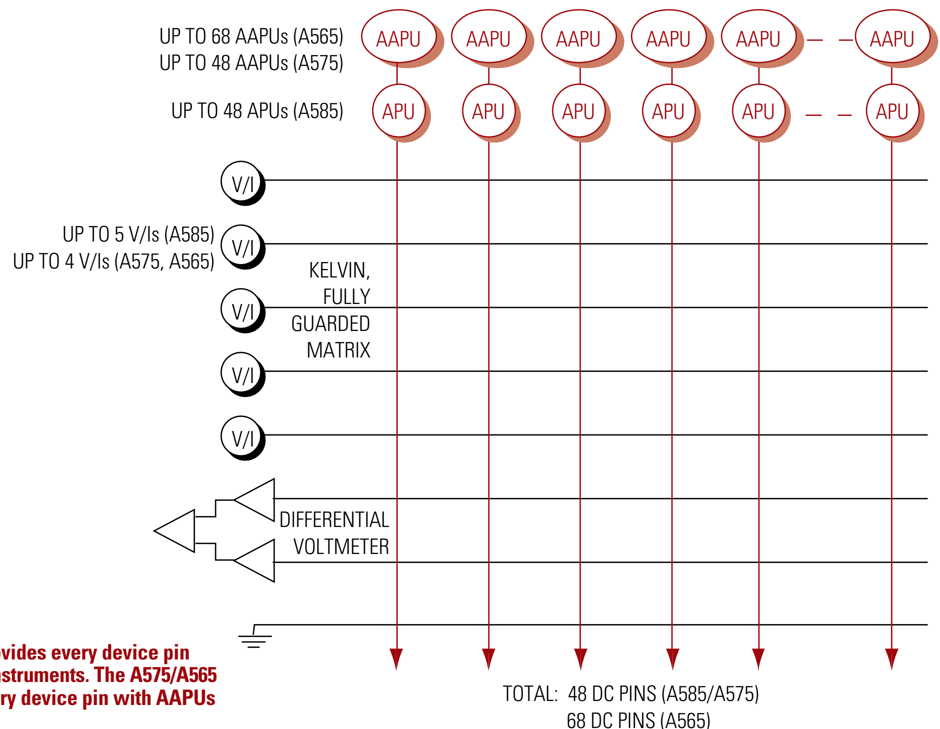


Figure 76
The A585 series dc matrix provides every device pin with APUs and standard dc instruments. The A575/A565 series dc matrix provides every device pin with AAPUs and standard dc instruments.

sources are four quadrant V/I instruments with solid-state switching for fast setup and low transients. Sources are calibrated under software control to an internal reference standard. With this reference standard, each V/I source can force and measure voltage accurate to within 0.05% and current accurate to within 0.1%. For high current requirements, these sources connect in parallel over the matrix or on the DIB.

The dc source can also connect to the DUT in a direct mode. The system can be configured to contain four additional sources on the A585 (3 sources for the A565 and A575) that connect directly to the Device Interface Board. These DUT sources access the device through the DUTSRC path. A disconnect card located in the test head allows software to disconnect the device from the sources.

Through the Universal Bus, the V/I sources access the Measure Bus and the Modulation Bus. The system voltmeter makes the voltage and current measurements. The source provides the current to voltage conversion, and the Modulation Bus provides the ability for an ac or dc source to modulate a device power supply for power supply rejection ratio tests. Refer to figure 77 for an overview of the capabilities of the dc instruments.

Differential Voltmeter

The dc matrix Differential Voltmeter can operate in a single-ended mode also and includes the following features:

- Dual ±60 V single-ended voltmeters or a 120 V differential voltmeter
- Sample and difference module with xl, x10, x100 gain
- Noise reduction filter
- Driven guards with matrix connectivity

The measurement system is calibrated against the same internal reference standard used for the sources. Meter accuracy is within 0.05%.

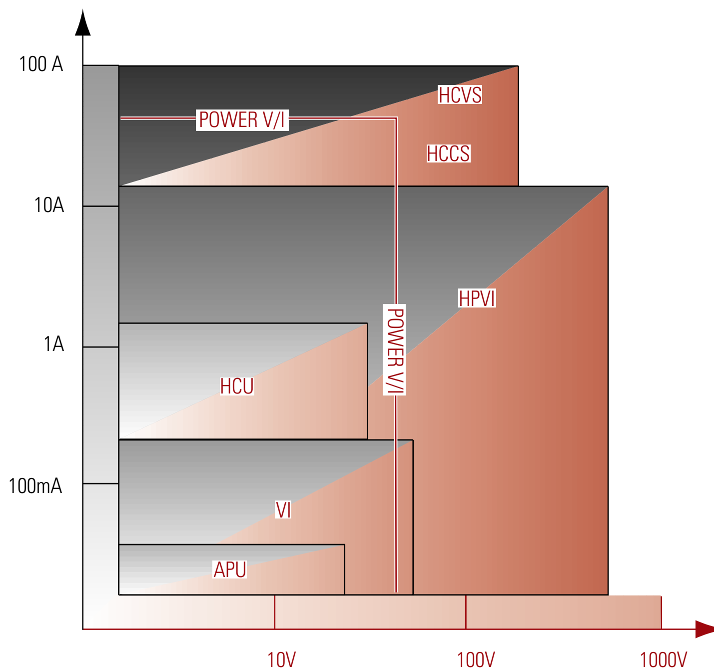


Figure 77
A full spectrum of V/I instruments address the most demanding applications.

Analog Pin Unit

The A585 Analog Pin Unit (APU) can be configured to contain a total of 48 pins in increments of three pins. These V/Is are also four-quadrant instruments that measure current while forcing voltage, and measure voltage while forcing current. The V/I range is ±24 V, ±30 mA.

Each group of 24 APUs is controlled by an MC68000 microprocessor residing on a dedicated controller board that also contains 64 bytes of RAM and 64 bytes of EPROM. The memory stores instrument setup and control instruction states and can capture voltage readings from the local 12-bit measurement A/D converter connected to an APU measurement bus. The converter can make measurements at a 125 kHz rate, and the controllers can operate in parallel for maximum test throughput. The APUs also interface to the Modulation and Measure Buses in order to access the system meter.

Advanced Analog Pin Unit

The A575 and A565 can be equipped with a 30 V Advanced Analog Pin Unit (AAPU) as shown in figure 78. Up to 48 AAPUs (A575) or 68 AAPUs (A565) can be configured in increments of four pins. These V/Is are four-quadrant instruments that measure current while forcing voltage, and measure voltage while forcing current. The AAPU has a programmable ±30 V source and a programmable current clamp to ±30 mA in the force voltage mode. As a programmable current source, the AAPU has a programmable ±30 mA force current, with programmable compliance voltage to ±30 V. The AAPUs are implemented as rider boards that install on the dc crosspoint matrix boards. The AAPUs provide direct connection to the Measure Bus.

High Current Unit

The 60 V/200 mA sources can be paralleled to provide greater currents for mixed-signal devices in high pin count packages. Additionally, the A585/A575/A565 series can be configured with four High Current Units (HCU) operating in four quadrants with the ability to force and measure voltages over a range of ±30 V and ±1 A through the matrix.

The HCU can also be configured to connect directly through the DUTSRC path instead of through the matrix. In this mode, the HCU provides up to ±2 A and replaces the standard 60 V/200 mA V/I.

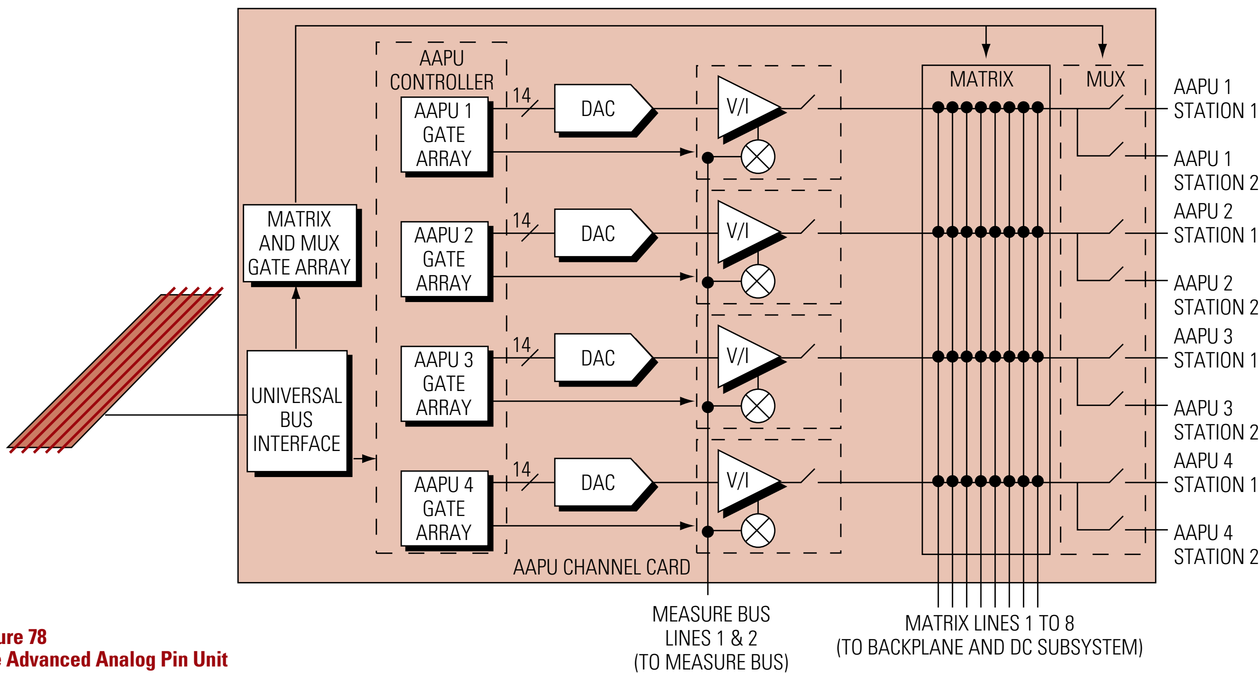


Figure 78
The Advanced Analog Pin Unit

Quad Power V/I

The Quad Power V/I provides four independent, fully floating power supplies. The supplies float to ±300 V above ground and operate in either 2- or 4-quadrant modes. Maximum output current from any supply is 30 A plulsed; however, for increased output capacity, the outputs can be paralleled. Maximum output voltage from any supply is 50 V; however, the supplies may be stacked for greater voltages.

PRECISION DC INSTRUMENTATION

Precision Multimeter Module

The Precision Multimeter Module (PMM) option provides high accuracy dc, ac, and resistance measurements for device test applications such as full scale gain and offset measurements on high precision A/D converters and high accuracy voltage measurements on system silicon. The PMM, which includes a mainframe module and a channel card in the test head, can also be used as a reference meter for calibrating analog instrumentation.
For the device to channel card path, the instrument provides numerous options including driven guard for low capacitance. The PMM can also access the dc matrix and the Test Head Analog Distribution System (THADS) Bus in the test head. Through these connections, the PMM has access to every device pin under software control including digital VLSI, analog, and dc pins. The PMM has a programmable resolution of 23 bits including sign and can make voltage measurements with better than 3 ppm accuracy.

Reference Source

The Reference Source is a low noise voltage source. Many devices such as precision ADCs, microcontrollers with on-board ADCs, and DACs require an externally generated reference voltage. The reference voltage must be extremely stable with very low noise, in order to accurately measure the linearity and noise performance of the converter.

The Precision Reference Source can generate up to ±11 V on one channel or, differentially, on two channels, ±11 V each with 17 bits of resolution. It has a rapid settling time of <2 ms to 1 ppm of final value for high throughput testing and remains stable to <5.5 µV of drift over 5 seconds, which is necessary when testing linearity of high resolution converters. The Reference Source has less than 3.5 µV rms noise over a 20 kHz range, which is required to accurately determine the device signal-to-noise ratio performance with the Precision Low Frequency Source and Precision Low Frequency Digitizer.

Quad Op Amp Loop

With the continued integration of Application Specific Standard Products (ASSP) in the consumer, communications, automotive, and instrumentation markets, high performance analog components are continually added to the system silicon. The components, which include precision operational amplifiers, analog switches, comparators and line drivers, require high performance instruments in the production environment where throughput and measurement guardbanding are critical for improved yield.

Many of the A585/A575/A565 series advanced analog instruments integrated into the Universal Bus architecture, provide synchronous measurements to a common, high performance meter.

The Quad Op Amp Loop (QOA) shown in figure 79 is used for gain, V_{OS}, and rejection ratio testing of operational amplifiers and for devices with on-board op amps. The QOA employs four parallel measurement

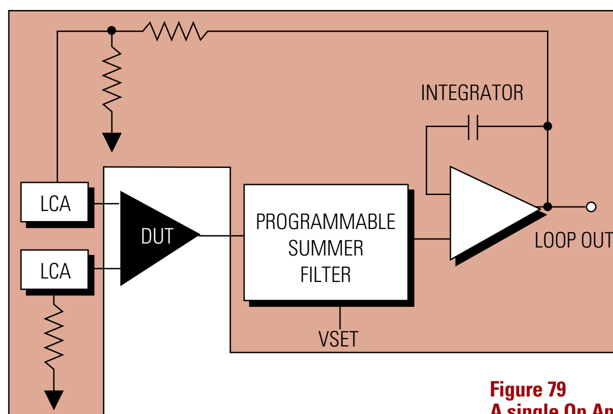


Figure 79
A single Op Amp Loop testing one component. Three wires are the only required connections.

loops, allowing measurement of all standard dc parameters. When making V_{OS} based measurements, the QOA provides ranges from 970 nV to 99 mV. Accuracy is 0.25% in x100 and x1,000 gains, and 0.5% in x10,000 gain setting. Each loop provides selectable internal gain of x100, x1,000, and x10,000 with switchable polarity. Input Vos nulling up to ±20 mV provides improved resolution for making AVOL, PSRR, and CMRR measurements.

Both continuity testing at 220 µA and solid-state switching for short-circuit current testing are provided. Built-in alarms detect device oscillation, loop saturation, and open loop conditions.

Although the Quad Op Amp Loop is a single board instrument in the test head, multiple boards can be added to handle additional parallel device testing. The QOA accesses the Universal Bus elements including the Trigger Bus, Measure Bus, and the Modulation Bus for complete operational amplifier testing.

Low Current Ammeter

The Low Current Ammeter (LCA) is a test head channel card instrument for bias and leakage current measurement of high performance Op Amps and MOS switches embedded on mixed-signal devices. The LCA depicted in figure 80 provides measurement capability down to the sub-picoAmp region and can act as a stand-alone instrument or as a companion instrument to the QOA. The LCA contains parallel I/Vs that operate in either resistive or integration mode when measuring ultra low currents.

In resistive mode, three ranges are available: 100 nA, 1 µA, and 10 µA. In integrate mode, additional ranges include l0 nA, 1 nA, 100 pA, and 10 pA. Measurements are made rapidly with an on-board commutator selector and multiplexer, which are synchronized by the Universal Bus.

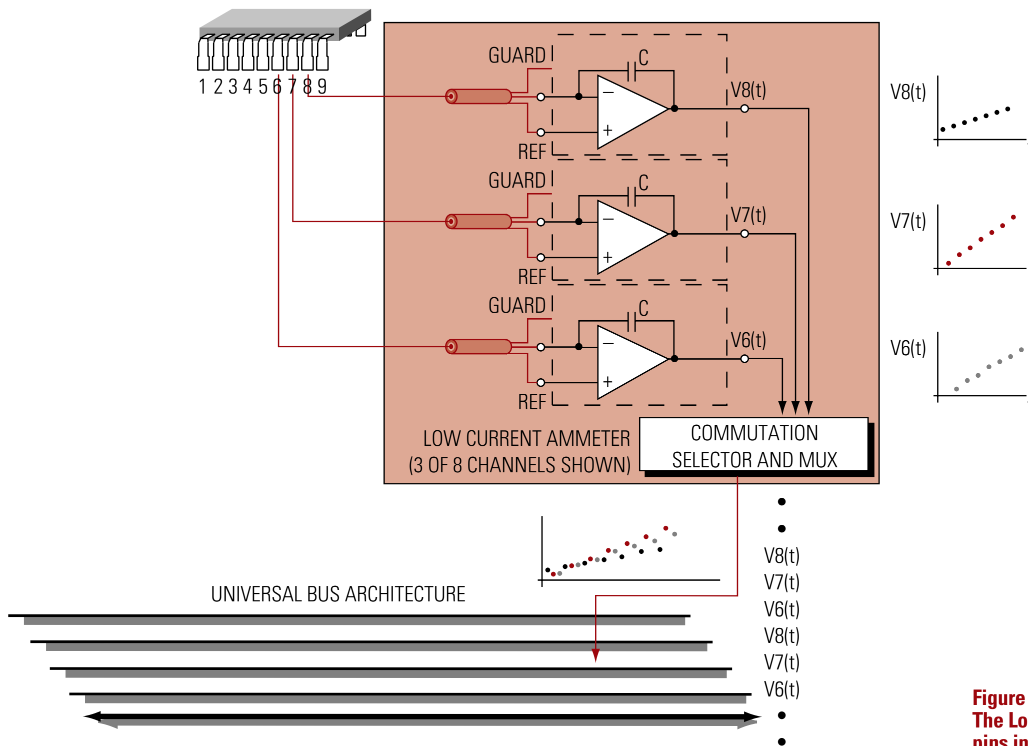


Figure 80
The Low Current Ammeter tests eight device pins in parallel.

The signal delivery path to the instrument is critical for successfully making low current measurements. The advanced mixed-signal test head provides a Teflon® insulated path to minimize leakage due to dielectric absorption.

The LCA interface includes the Universal Bus elements of the Measure Bus and the Trigger Bus.

Pulse Driver

Testing high speed Op Amps with very fast rise and settling time characteristics requires an input signal that is higher quality than the device itself. The Pulse Driver can generate pulses from 100 ns to 4 ms in width with a rise time <20 ns, settling to 1% of final value in less than 50 ns. The programmable swing of the driver is ±5.5 V.

This channel card-based instrument has multiple output signal paths to the DUT. A 50 Ohm RF connection provides a high quality signal path. A 95 Ohm analog signal path offering voltage swings to ±11 V with selectable 35 ns or 85 ns risetime and 250 ns or 100 ns settling time is available, as well as differential ECL outputs.

Pulse generation can be triggered from the Universal Bus through the Trigger Bus interface. See figure 81.

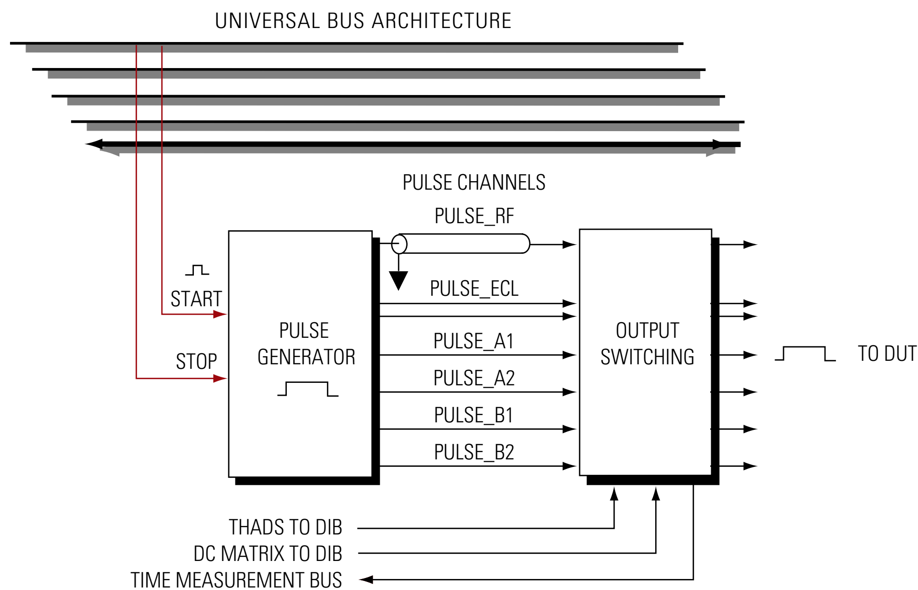


Figure 81
Multiple output channels are provided for the pulse driver.

SYNCHRONIZED POWER INSTRUMENTATION

A variety of high power voltage and current instruments used in automotive and power management test applications are available for use in the A585 and A565 series test systems. Designed by Teradyne, these instruments have:

- An optimized ATE environment strategy with fast switching and control for production test
- High performance that meets and exceeds the most difficult device demands
- Internal instrument protection that maximizes Mean Time Between Failures (MTBF) by preventing instrument failures caused by a bad device
- IMAGE software control, debug displays, and operating environment
- Intelligent software routines that prevent test programs from hot switching
- Crowbar circuits that provide additional protection

These mainframe-based instruments are shielded and enclosed with multiple signal interlocks to protect engineers, operators, and service personnel from accidental injury.

Internal system alarms help prevent system failures during debugging sessions. These include:

- Limit Alarms – occur if a voltage clamp or current clamp is reached
- Open Loop Alarms – occur when a control loop is unstable
- Overload Alarms – occur if excessive current is flowing in the instrument sense lead
- Over Voltage Alarms – occur in the event of overvoltage condition across the instrument output
- Heat Sink Alarms – occur if the thermal sensor on the internal heat sinks senses that a temperature is too high

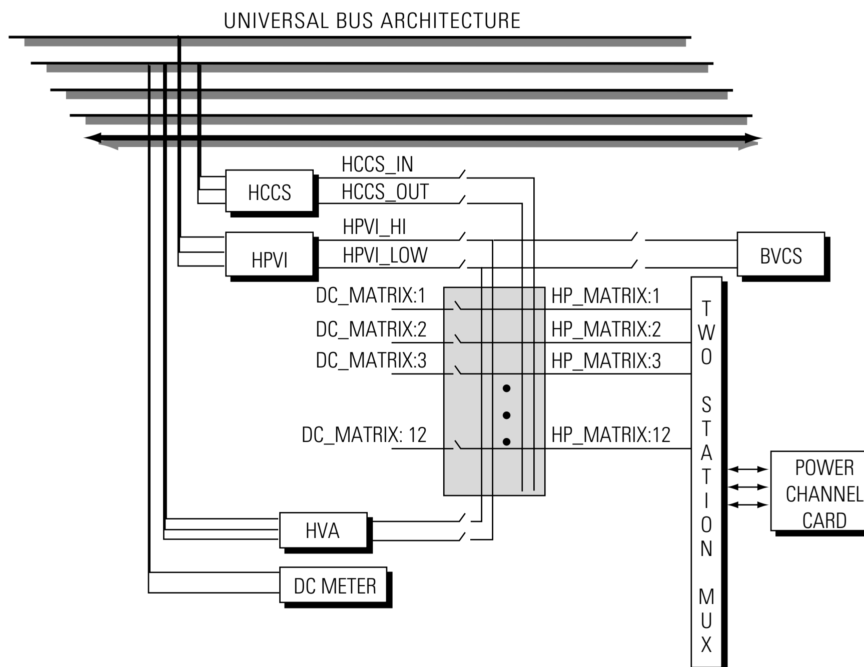


Figure 82
All power instruments can be two station multiplexed and interfaced to the Universal Bus Architecture.

- Temperature Warning Alarms – occur if a temperature shutdown level is being approached
- Over Current Alarms – occur if greater than 200 mA is flowing when making a range change, connect or disconnect
- Junction Temperature Alarms – occur if an instrument output transistor junction temperature becomes too high

The power instruments cover a full spectrum of voltage and current requirements ranging ±750 V and ±100 A. Refer to figure 76. These instruments access the Universal Bus architecture as illustrated in figure 82.

High Power V/I

The High Power V/I (HPVI) can force voltage and measure current, and force current and measure voltage over a range of 750 V and 10 A. It provides an auto crossover into the power sinking quadrant (+V, -I) and can rapidly discharge reactive loads. The instrument is fully floating. By reversing its connection signals, it can also operate in the -V quadrants.

High Power Matrix

The standard dc matrix handles 1 A through its relays and signal paths. The optional High Power Matrix (HPM) supports an additional 4 lines and 12 pins. See figure 83. Two lines support 40 A (80 A pulsed) and two support 20 A (40 pulsed). Each pin on the 20 A dc line supports up to 5 A dc or up to 10 A pulsed. Each pin on the 40 A dc line supports up to 10 A dc or up to 20 A pulsed. The maximum voltage rating is 1000 V. Connections to the standard dc matrix are protected with 1 A fast-blow fuses and 65 V trip point crowbar circuits. A second HPM provides a total of 24 high power matrix pins to the DUT. Pulsed power is used for testing devices that require high current and device package protection from heat, which could alter the device characteristics.

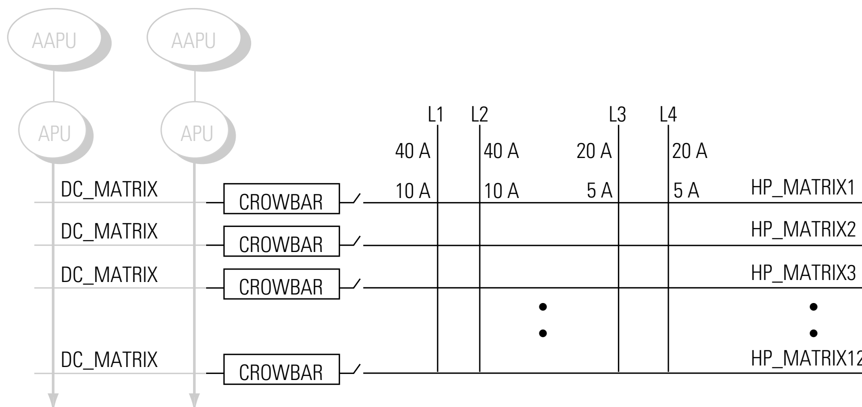


Figure 83
The High Power Matrix extends the standard system matrix and provides the ability for power instruments to access multiple device pins while reducing load board electronics.

High Current Current Source

The High Current Current Source (HCCS) is commonly used for RdsON and Vcesat measurements or in applications that require a large current load. It can source or sink current up to 100 A at 14 V in pulsed mode and independently measure voltage or current. In non-pulsed mode, it is capable of 25 V and 15 A, continuous. When operating as a load, it can have as much as 100 V across and float to 1000 V referenced to ground. In either source or load mode, the HCCS connects to the DIB through the high power matrix.

High Current Voltage Source

The High Current Voltage Source (HCVS) is another instrument for applications requiring pulsed power up to 12 V at 100 A or 110 V at 25 A. This instrument is commonly used in automotive applications where the automotive battery is simulated to test devices such as high side switches. The HCVS forces voltage and measures current. It floats with reference to ground. HCVS provides auto crossover to the power sinking quadrant (+V, -I) and can rapidly discharge reactive loads. The HCVS connects to the DIB through the high power matrix.

High Voltage Ammeter

The High Voltage Ammeter has full floating capability for performing leakage measurements and H-bridge testing. Leakage current is minimized in the signal path by employing a driven guard design. The HVA connects to the DIB through the High Power Matrix. This instrument measures current up to 100 mA and provides ±20 nA accuracy. It can float to 1000 V common mode voltage.

Breakdown Voltage Current Source

The Breakdown Voltage Current Source (BVCS) makes very low current breakdown voltage measurements. The BVCS is a test head-based channel card used in conjunction with the High Power V/I. The instrument can float to the voltage level of the sourcing instrument with a minimum current forcing range of 10 µA. The BVCS also has a voltage source mode for leakage measurements and contains both voltage and current metering capability.

Production Interface

Because of the greater integration from both the analog and digital ends of the spectrum, today's devices demand a wide range of mixed-signal test instrumentation performance. This wide range of test instrument performance requires a test head that can provide a variety of signal paths between the device and system instrumentation. The A585/A575/A565 Series of Advanced Mixed-Signal Test Systems meets these increased demands with two implementations of test head and test head/mainframe interconnections, each tailored to the test system capabilities that they support. Instrument channel card electronics close to the device and signal delivery paths from the channel card to the device interface board provide a full spectrum of instrument performance.

Each instrument requires a unique signal path in order to guarantee performance at the DUT:

- Ultra-low (sub-picoAmpere) current measurements require conductors with very low dielectric absorption and triboelectric effects. This is provided by a Teflon-isolated delivery path
- To minimize resistance, high voltage and current instruments need heavy gauge conductors
- Precision Low Frequency Source requirements exceed 115 dB harmonic distortion. To guarantee this exceptional performance, signals travel through shielded, twisted pairs from the channel card to the interconnections of the interface area
- The 25/50/100/200 MHz digital signals travel through a 50 Ohm coaxial environment
- RF and very high frequency waveforms travel through a 50 Ohm semirigid coax conductor

To meet the instrument specifications and reduce application complexity, the advanced mixed-signal test head features include:

- Signal paths custom-configured for each instrument type
- Guaranteed instrument performance at the device interface area
- Channel cards with programmable flexibility, minimizing the amount of necessary applications circuitry
- Device interface area with maximum space for users to add their own circuitry
- Ability to dock to a variety of handlers and probers

DIRECT-DOCKING: ADVANCED MIXED-SIGNAL TEST HEAD

The A585 Advanced Mixed-Signal Test System can accommodate up to 192 digital I/O pins, and the A575 can accommodate up to 128. Both can be configured with up to 40 analog pins and a minimum of 48 dc pins. A total of 384 shielded Iso-Pin connections can connect to the DUT.

The left side of the test head has 24 slots for digital channel cards, the right has 15 for analog instrumentation channel cards. The remaining slots contain utility support functions, dc

matrix, dc resource, and time measurement support. Figure 84 depicts a typical channel card configuration.

The digital and utility support function slots are fixed. The configurable analog slots accommodate:

- High performance analog instrumentation channel cards
- High performance advanced analog instrumentation
- User designed channel cards
- Relay disconnect cards for multiplexing a single instrument to multiple device pins

Configuration Board

The configuration board (signal delivery board) connects the channel cards to the Iso-Pin connections. See figures 85, 86 and 87. Two configuration boards contact the channel cards and the test head Iso-Pins. The digital configuration board connects the digital pins to the Iso-Pins and carries the 5O Ohm coaxial wire. The analog configuration board connects the analog channel card signals to the Iso-Pins and contains the appropriate signal paths for the system and test head instrumentation.

It is the configuration board that provides the ability to adapt the signal delivery system to a wide range of instrumentation without requiring a different interface environment. Standard configura-

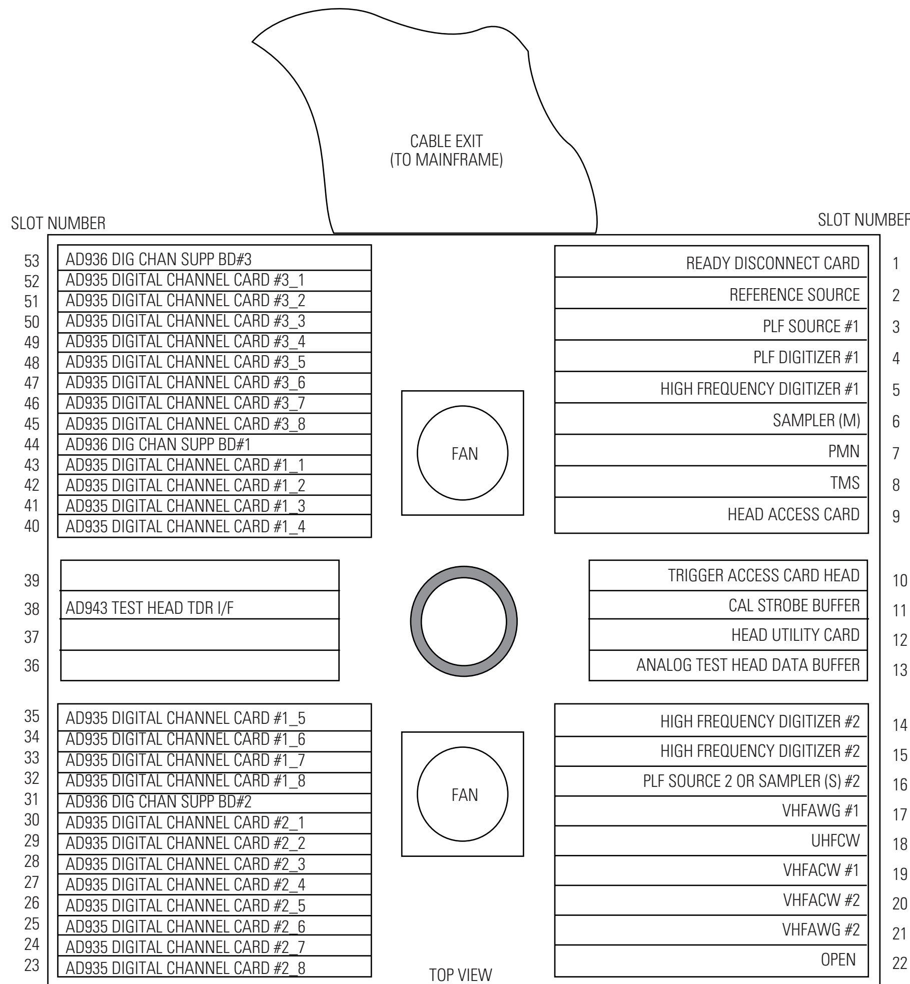


Figure 84
Direct-docking test head layout with a typical channel card configuration

tion boards designed by Teradyne accommodate most typical instrument configurations.

Iso-Pin Connections

The Iso-Pins are spring pins that connect the configuration board to the device interface board (DIB). The Teradyne patented Iso-Pin design maintains a shielded environment to the DIB and provides a 40-50 dB crosstalk reduction between the analog and digital signals over conventional, unshielded environments. See figure 86 and 87.

Device Interface Boards

A variety of device interface boards accommodating a number of unique interface schemes are available for use on the test floor. The standard board provides over 60 square inches for user-specified applications interface circuitry. Typically, the interface board carries only the appropriate bypass capacitors required by the device and the signal connections from the DUT pin to the tester Iso-Pin. The channel cards eliminate the need for applications circuitry required by a conventional test system.

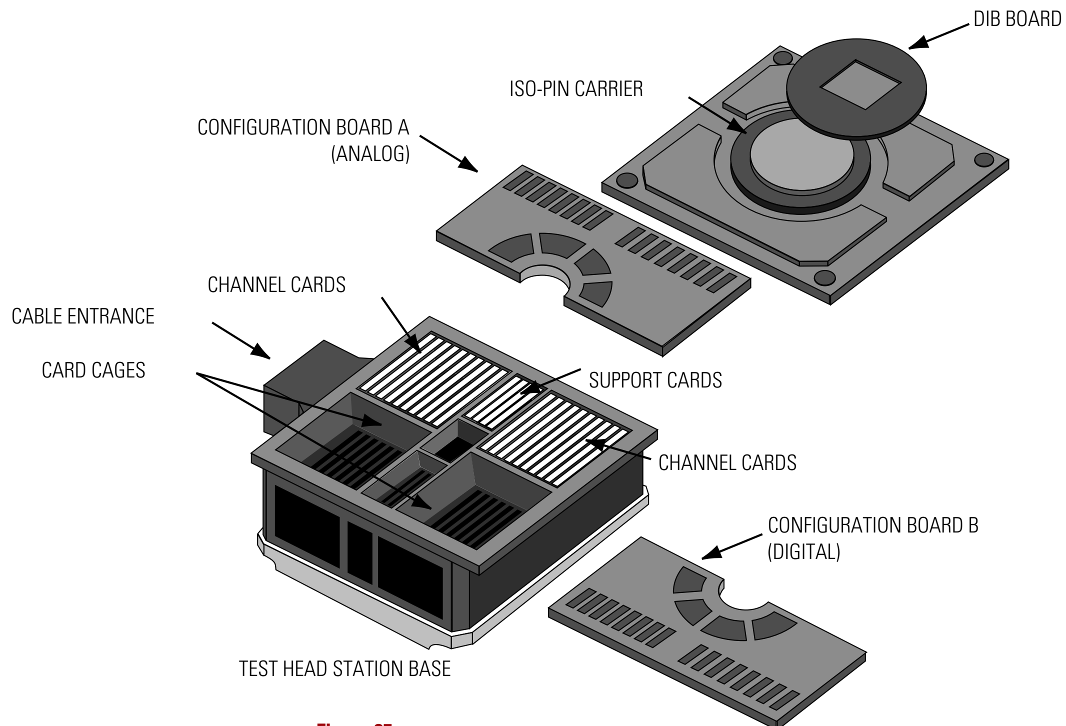


Figure 85
Exploded view of the A585 Series Advanced Mixed-Signal test head elements

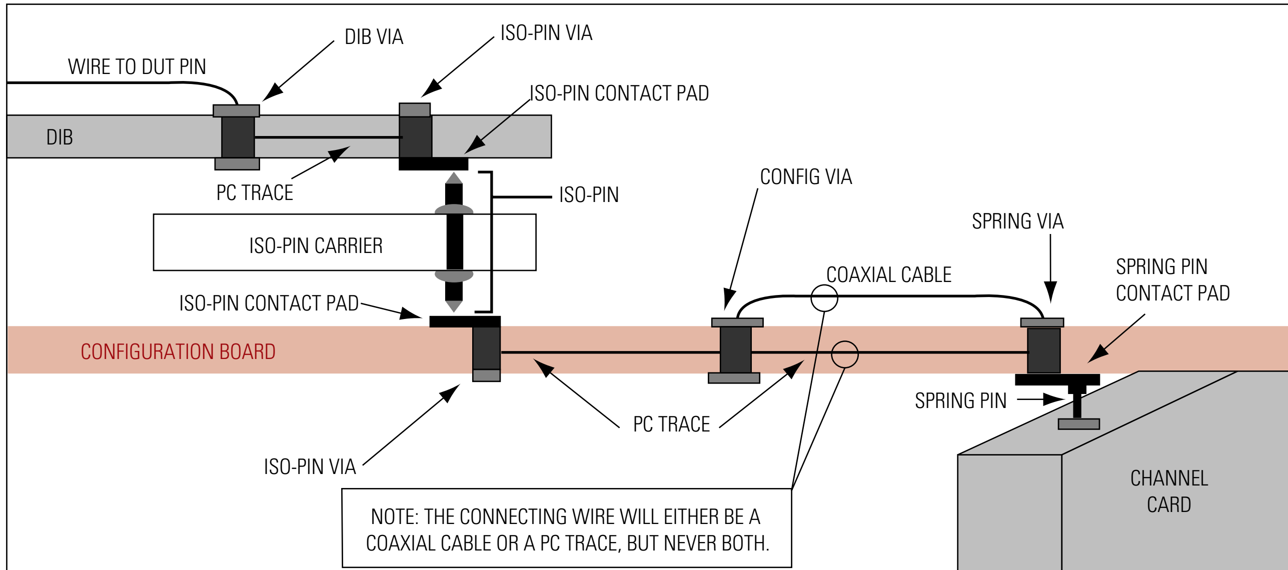


Figure 86
The Configuration Board carries the required signals for all the instruments.

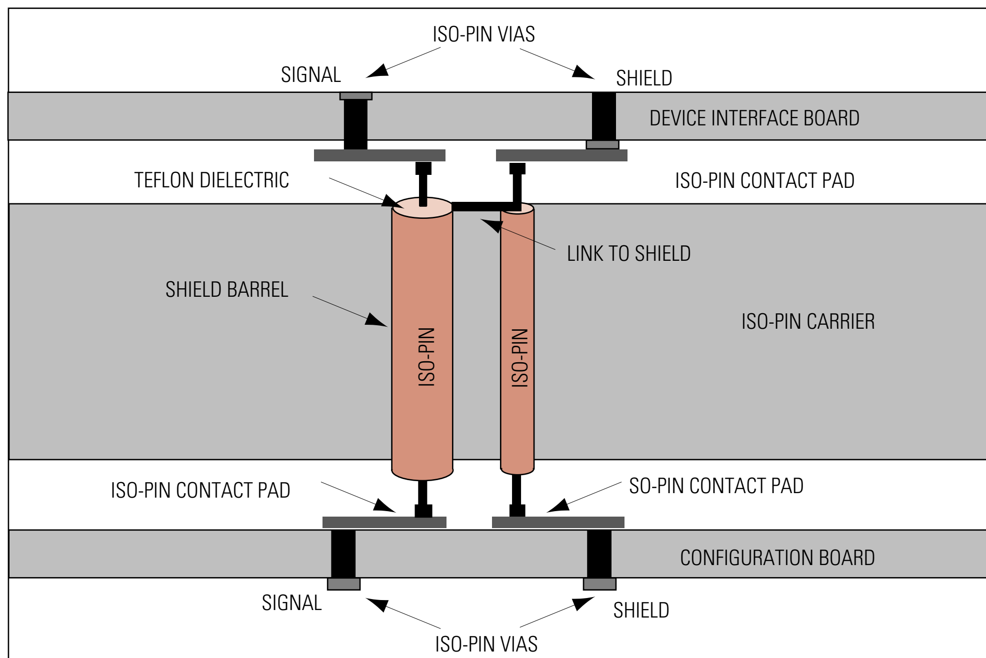


Figure 87
The Teradyne patented Iso-Pins deliver full instrument performance in a shielded environment while withstanding the rigors of the production floor.

CABLE INTERFACE: PRODUCTION ANALOG TEST HEAD (PATH II)

The A565 Advanced Mixed-Signal Test System can also be configured with the Production Analog Test Head (PATH II). The test head has eight slots for digital channel cards and seven for analog instrumentation channel cards and two for power V/I channel cards. The remaining slots contain utility support functions, dc matrix, dc resource, and time measurement support. Figure 88 depicts a typical channel card configuration.

The PATH II test head is much smaller than the direct-docking Advanced Mixed-Signal Test Head. See figure 89. Because it eliminates the need for precision mechanical docking assemblies, the PATH II head reduces cost both in terms of materials and floor-space, optimizing it for testing highly cost-sensitive devices. Connection to test-floor equipment is achieved via a cable interface between the configuration board and the device

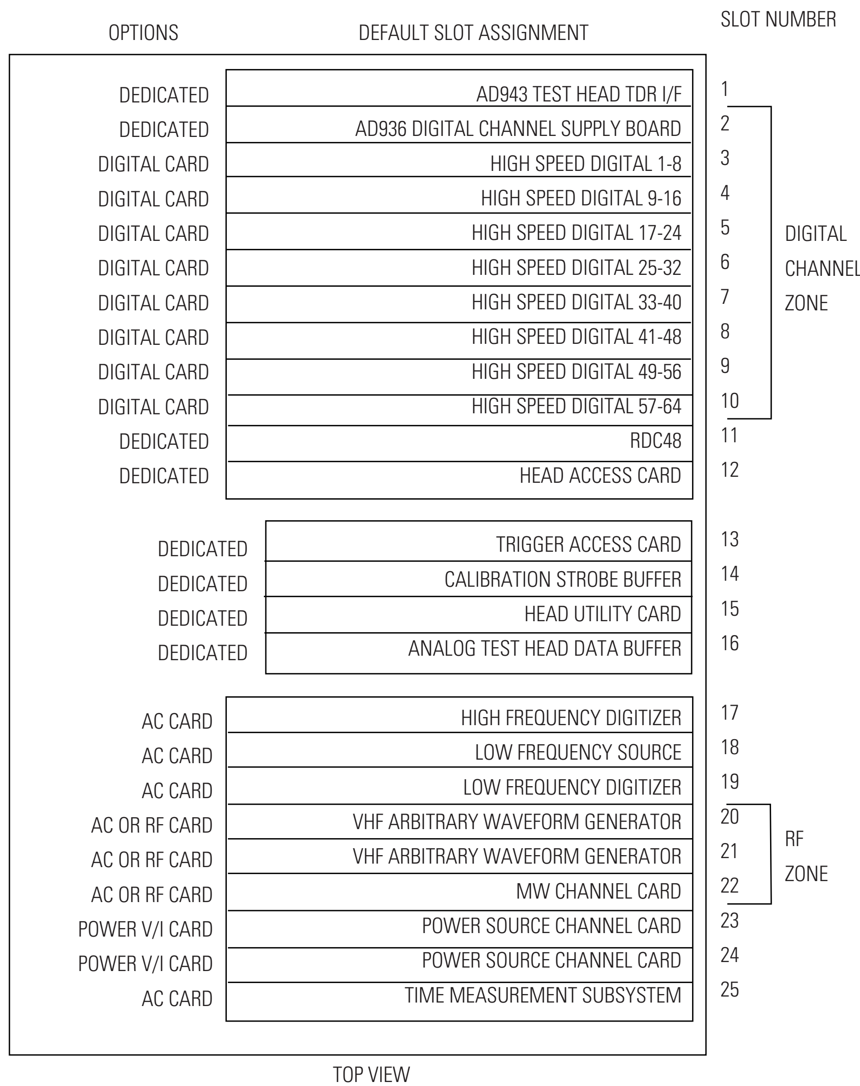


Figure 88
PATH II test head layout with a typical channel card configuration

board. See figure 90. Either the cable interface or the configuration board/ cable assembly can be quickly and easily changed.

The PATH II configuration supports 72 dc channels, 64 digital channels, and has eight analog channel card slots for precision ac and other head-based analog instruments. There are two time measurement channels in PATH II. The instruments are specified at the end of 39" (1 meter of cable). Physically the PATH II measures 28" wide by 18" deep by 18" high (71 cm x 45 cm x 45 cm).

The PATH II is software compatible with the Advanced Mixed-Signal (AMS) test head. Programs developed on PATH II can be leveraged to other

Figure 89
The PATH II cable interface easily connects to test floor equipment like the Tokyo Seimitsu prober shown here, without requiring expensive, custom-designed docking assemblies.

A585/A575/A565 series test systems by attaching the cable interface to the device interface board on the Advanced Mixed-Signal test head.

HANDLER AND PROBER INTERFACING

Appropriate mechanical, electrical and communications interfaces must integrate with handlers and probers on the production floor. A wide variety of handlers and probers are supported by the A585, A575 and A565 Mixed-Signal Test Systems.

The A585 and A575 systems use a direct docking method of interfacing that minimizes signal path length between the silicon and the tester channel. The robust design of the docking mechanics withstands the rigors of the production floor.

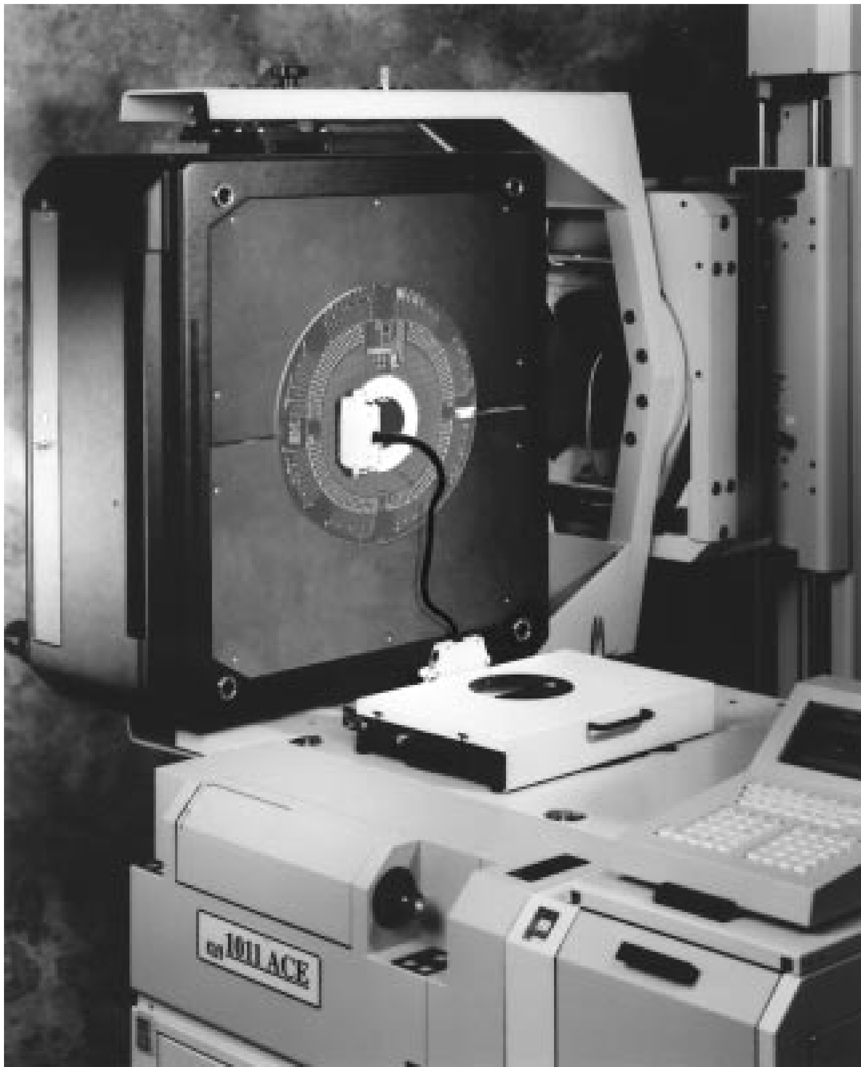


Figure 90
PATH II Configuration Board installed in an A585/A575 Advanced Mixed-Signal Test Head allows one test system in engineering to be used to develop test programs for AMS or PATH test heads.

System Configurations

A summary of the primary system model configurations within the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems is provided below. The A585/A575/A565 series models are designed to be compatible subsets of one another, sharing the same instrumentation, but differing in baseline configurations. Test programs developed on one can be implemented on the other. Please refer to table 4 that follows for a tabular comparison of each system, and to figures 91, 92 and 93 for a footprint comparison.

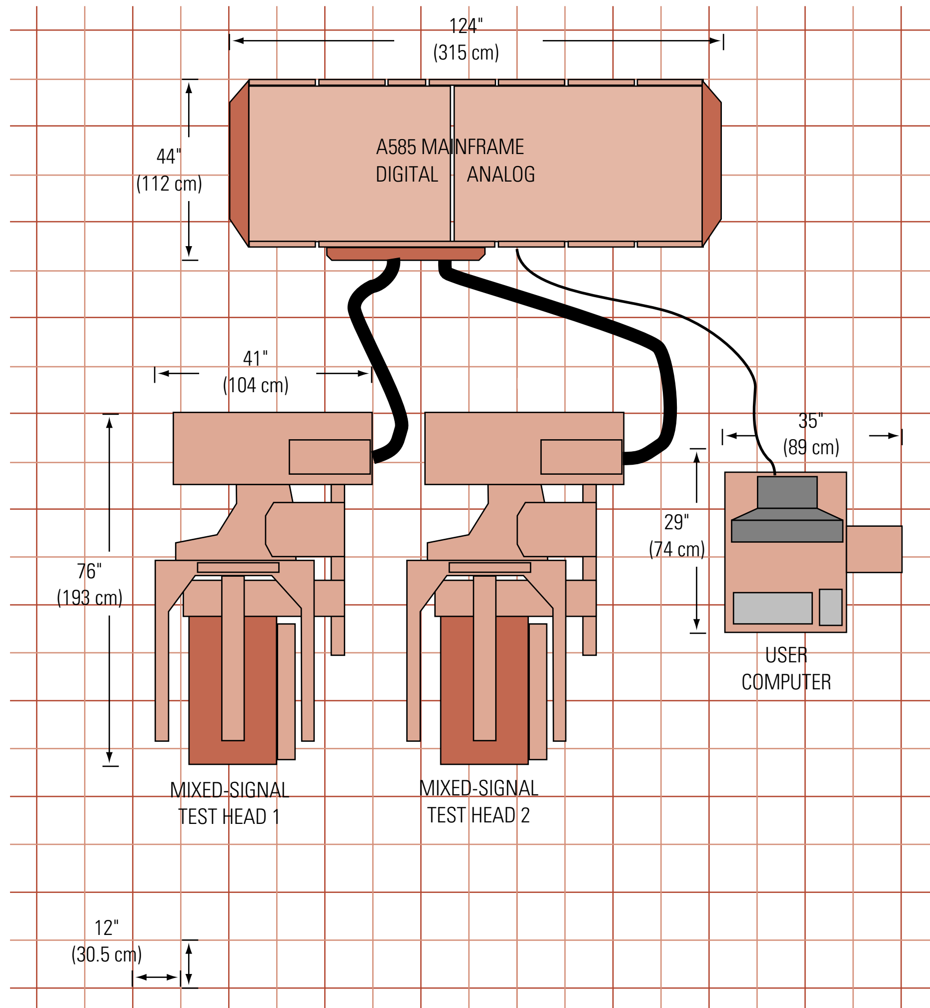


Figure 91
A585 Footprint

TEST SYSTEM FOOTPRINT

The A585/A575/A565 instrumentation provides high performance and reliability in a compact system footprint. The highly integrated E/MOS design of the digital pins helps to minimize the size of the system by reducing the number of printed circuit boards and backplanes. A fully configured 192 pin A585 test system mainframe occupies only 37 square feet. A fully configured 128 pin A575 test system mainframe occupies only 23 square feet, and the A565 with 64 digital channels, occupies 17 square feet.

The test systems can be configured with two direct-docking AMS test heads. See figures 91 and 92. Mainframe instrumentation is multiplexed

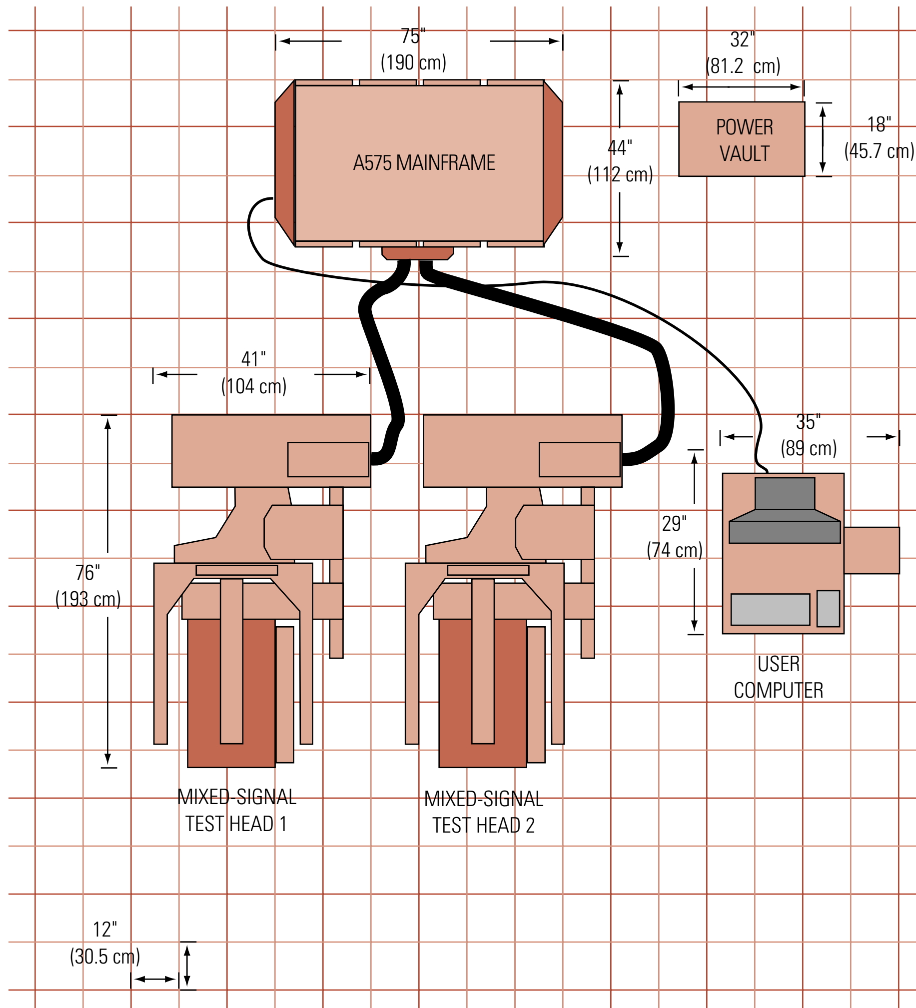


Figure 92
A575 Footprint

to both stations, allowing for up to twice the test throughput for the incremental cost and floorspace requirements of the second test head. Each head can have a different slot assignment and a different number of cards. For example, if the first head has 192 digital pins, the second head can be targeted for devices with lower pin count, thus requiring fewer pins.

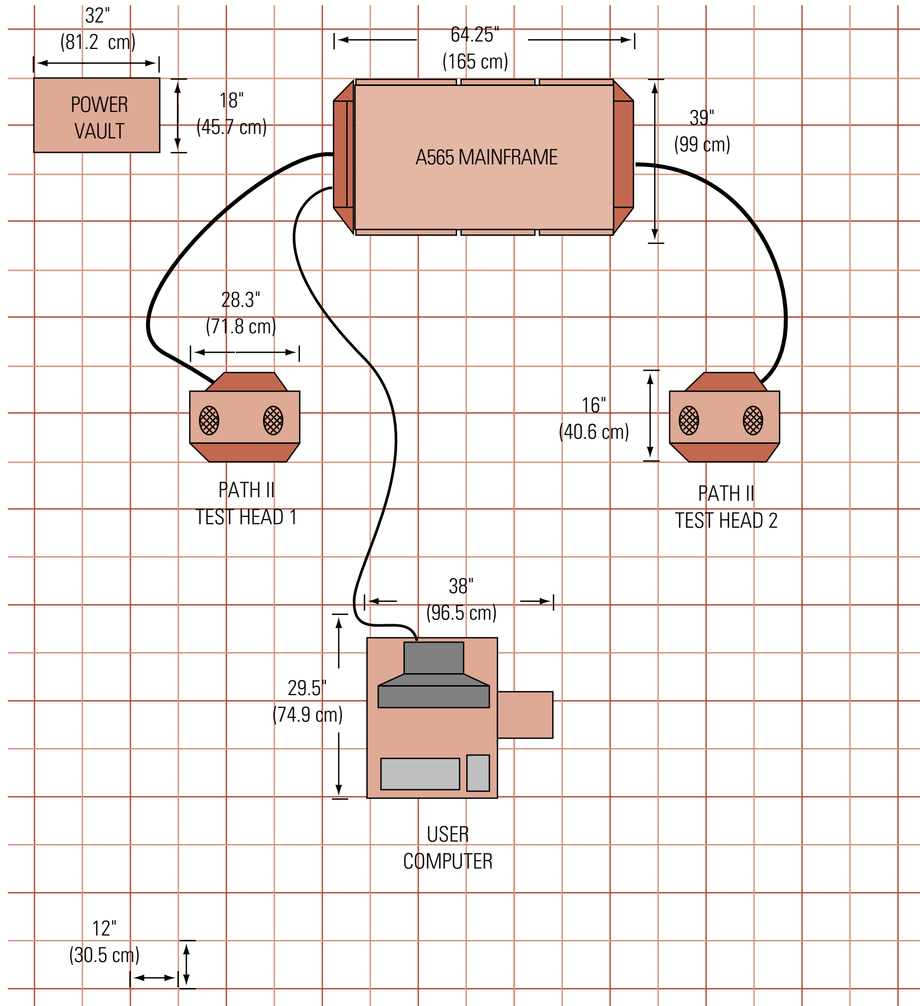


Figure 93
A565 Footprint

A585 ADVANCED MIXED-SIGNAL TEST SYSTEM

The A585 is the high pin count model of the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems. The A585 is able to support two Advanced Mixed-Signal test heads, with virtually all available options. The A585 can be configured to support both disk drive device and RF device testing in a single test head, with some limitations on expansion in that test head. Over time, as needs change, instruments can be added, moved and a second test head can be installed.

A575 ADVANCED MIXED-SIGNAL TEST SYSTEM

The A575 is a lower-cost, reduced configuration version of the A585. It features the precision and flexibility of the A585, but with limitations on the total digital pin count.

A565 ADVANCED MIXED-SIGNAL TEST SYSTEM

The A565, another member of the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems, is designed for testing high volume, low ASP devices. The A565 features the performance of the A585 instrumentation in a system that can be more flexibly configured for test applications highly sensitive to cost. Like the A585 and A575, the A565 supports parallel testing to further increase throughput and reduce cost-to-test. The A565 uses the PATH II test head or optional advanced mixed signal test head.

The A565 base configuration supports analog/dc parametric testing. The first extension of A565 configuration adds either the pre–cision ac instrumentation and associated card cage and power supply, or the digital instrumentation and its associated card cage and power supply. The A565 can be further extended to be configured as a mixed-signal test system, with additional mixed-signal capabilities.

Feature and Specification Comparison among the A585/A575/A565 Series Test Systems

SUBSYSTEM			A585	A575	A565
DC Instrumentation					
60 V/200 mA V/I					
Matrix			5 max.	4 max.	4 max.
DUT_SRC			4 max.	3 max.	3 max.
Analog Pin Unit			0	N/A	N/A
Advanced Analog Pin Unit			N/A	0	0
Digital Instrumentation					
Maximum Pin Count			192	128	64
Data Rate (MHz)					
	PATH II	HSD25	—	—	25/50
	AMS	HSD50–25	25/50/100	25/50/100	25/50/100
		HSD50–51	50/100/200	50/100/200	50/100/200
		HSD50–50	50/100/200	50/100/200	50/100/200
Top Speed (Mbps)					
	PATH II	HSD25	—	—	50
	AMS	HSD50–25	100	100	100
		HSD50–51	200	200	200
		HSD50–50	200	200	200
Edge Placement Accuracy					
	PATH II	HSD25	—	—	±1 ns
	AMS	HSD50–25	±500 ps	±500 ps	±500 ps
		HSD50–51	±500 ps	±500 ps	±500 ps
		HSD50–50	±350 ps	±350 ps	±350 ps
Pattern Depth					
	PATH II	HSD25	—	—	64 K/1 Meg option
	AMS	HSD50–25	1 Meg	1 Meg	1 Meg
		HSD50–51	510 K/1 Meg option	510 K/1 Meg option	510 K/1 Meg option
		HSD50–50	1 Meg	1 Meg	1 Meg
Second Sequencer			Opt.	Opt.	N/A
Dual Sequence Function			Full	Limited Asynch DSI/O	N/A
Digital Signal I/O (Serial)			Opt.	Opt.	Opt.
Vector Bus Memory for SCAN			Opt.	Opt.	N/A
140 MHz Channels			Opt.	Opt.	N/A
Superclock			Opt.	Opt.	N/A
Super Speed Serial Pins			Opt.	Opt.	N/A
Time Jitter Digitizer			Opt.	Opt.	N/A
Relative Analog Mainframe Space Units			40	22	18/49
Test Head					
PATH II		N/A	N/A	S	
Advanced Mixed Signal			S	S	Opt.
Physical					
Floor Space (sq. ft.)					
	Mainframe		37	23	17
	Test Head Plus Manipulator		22	22	3
Cabinets			2	1	1

S = Standard;
Opt. = Available Optional;
N/A = Not Available for this system

Please contact your Teradyne salesperson for detailed configuration information.

Table 4
Feature and Specification Comparison among the A585/A575/A565 Series Test Systems

Instrument Specifications

KEY INSTRUMENT SPECIFICATIONS AND FEATURES

Key specifications and features are provided here for each of the instruments presently available for the A585/A575/A565 Series of Advanced Mixed-Signal Test Systems. These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

DIGITAL INSTRUMENTATION

High Speed Digital (HSD25)

Feature	Specification
Maximum channel count	64 channels
Vector rate (non-multiplexed)	
Basic vector rate	25 MHz
Single cycle I/O	50 MHz
Dual drive	50 MHz
Minimum vector rate	5 kHz
Pattern depth	64 K; 1 Meg optional
Pattern depth @ single cycle I/O	128 K; 2 Meg with option
Pattern depth @ dual drive	128 K; 2 Meg with option
Keep alive pattern memory	16 vectors
History memory	4 K vectors
Cycle counter	32 bits
Digital signal source memory	64 K x 20 bits
Digital signal capture memory	1 Meg x 20 bits
Edge placement accuracy	±1 ns
Edge resolution	78 ps
Edges per pin	6 (dl, d2, d0, d3, rl, r2)
Edge sets per edge per pin	32
Global timing sets	1,023
Drive formats	nrz ,nrzc, rz, rzc, ro, rocl, cs, csc, clkhi, clklo, fhi, flo, off, drvclkhi, drvclklo, drvhi, drvlo
Compare formats	cmplo, cmphi, cmplog, cmpmid, cmppat, cmpmask, cmpoff, rcvhi, rcvlo, rcvmid, rcvmask
Driver characteristics (with cable)	
V_{IH}/V_{IL} range	-2 V to +7 V
Resolution	1 mV
Output impedance	50 Ohm
Minimum pulse width (3 V swing)	10 ns
Rise/fall time (3 V swing)	< 5 ns
Rise/fall time (9 V swing)	< 10 ns

High Speed Digital (HSD25) (continued)

Feature	Specification
Comparator characteristics (with cable)	
V_{OH}/V_{OL} range	-2 V to +7 V
Resolution	1 mV
Input impedance @ dc	4 MOhm
Transmission line characteristics	7.0 ns delay @ 50 Ohm
Capacitance	<2 pF
Minimum pulse width detection	12 ns @ 500 mV overdrive
Dynamic load characteristics	
I_{OH}/I_{OL} range	50 mA
Resolution	5 µA
Vcp range	-2 V to +7 V
Vcp resolution	1 mV
I/O channel termination mode	50 Ohms
Per pin parametric measure unit characteristics	
Voltage forcing/measuring	-2 V to +7 V
Voltage forcing resolution	275 µV
Voltage forcing accuracy	±(0.16% + 14 mV)
Voltage measuring resolution	3.66 mV
Voltage measuring accuracy	±(0.43% + 18 mV)
Current forcing	±2 mA, ±200 µA (2 ranges)
Current measuring	±2 mA, ±200 nA (5 ranges)
Current measuring resolution	
±200 nA range	293 pA
Current measuring accuracy	
±200 nA range	±(1.4% + 2.1 nA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Speed Digital (HSD50-50)

Feature	Specification
Maximum channel count	192 channels
Vector rate (non-multiplexed)	
Basic vector rate	50 MHz
Single cycle I/O	100 MHz
Dual drive	100 MHz
Vector rate (multiplexed)	
Basic vector rate	100 MHz
Dual drive	200 M bits
Minimum vector rate	Approx. 5 kHz
Pattern depth @ basic vector rate	1 Meg
Pattern depth @ single cycle I/O	2 Meg
Pattern depth @ dual drive < 100 MHz	2 Meg
Pattern depth @ multiplexed mode	2 Meg
Pattern depth @ multiplexed, dual drive	4 Meg
Keep alive pattern memory	16 vectors
History memory	4 K vectors
Cycle counter	32 bits
Digital signal source memory	64 K x 20 bits
Digital signal capture memory	1 Meg x 20 bits
Edge placement accuracy	±350 ps
Overall tester accuracy	±500 ps
Edge resolution	78 ps
Fine edge resolution control	19 ps
Edges per pin	6 (dl, d2, d0, d3, rl, r2)
Edge sets per edge per pin	32
Global timing sets	1,023
Drive formats	nrz ,nrzc, rz, rzc, ro, rocl, cs, csc, clkhi, clklo, fhi, flo, off, drvclkhi, drvclklo, drvhi, drvlo
Compare formats	cmplo, cmphi, cmplog, cmpmid, cmppat, cmpmask, cmpoff, rcvhi, rcvlo, rcvmid, rcvmask
Driver characteristics	
V_{IH}/V_{IL} range	-4 V to +7 V (3 ranges)
Resolution	1 mV
Output impedance	50 Ohm
Minimum pulse width	< 5 ns
Rise/fall time (3 V swing)	1.35 ns ±500 ps
Rise/fall time (5 V swing)	2.20 ns ±500 ps

High Speed Digital (HSD50-50) (continued)

Feature	Specification
Comparator characteristics	
V_{OH}/V_{OL} range	-4 V to +7 V (3 ranges)
Resolution	1 mV
Input impedance @ dc	4 MOhm
Transmission line characteristics	3.0 ns delay @ 50 Ohm
Capacitance	<2 pF
Minimum pulse width detection	4 ns @ 500 mV overdrive
Dynamic load characteristics	
IOH/IOL range	50 mA
Resolution	5 µA
Vcp range	-4 V to +7 V (3 ranges)
Vcp resolution	1 mV
I/O channel termination mode	50 Ohms
Per pin parametric measure unit characteristics	
Voltage forcing/measuring	-4 V to +7 V (3 ranges)
Voltage forcing resolution	275 µV
Voltage forcing accuracy	±(0.16% + 14 mV)
Voltage measuring resolution	3.66 mV
Voltage measuring accuracy	±(0.43% + 18 mV)
Current forcing	±2 mA, ±200 µA (2 ranges)
Current forcing resolution (±200 µA range)	22 nA
Current forcing accuracy (±200 µA range)	±(0.2% + 1.7 µa)
Current measuring	
Current measuring resolution (±200 nA range)	293 pA
Current measuring accuracy (±200 nA range)	±(1.4% + 2.1 nA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Superclock (SCL)

Feature	Specification
Drive-only clock with differential output signal	
Programmable frequency	
Programmable clock pulse duty cycle	
Programmable voltage levels	
Requires dedicated PTS frequency synthesizer in mainframe	
Frequency range	50 MHz to 400 MHz
Frequency resolution	1 Hz
Frequency accuracy	1 ppm + 1 ppm/year
DC output voltage (V_{IH}/V_{IL}, no load)	
Levels	–2.0 V to +5.0 V
Resolution	1.22 mV nominal
Maximum voltage swing	
50 MHz to 100 MHz	5 V_{PK-PK}
100 MHz to 400 MHz	3.3 V_{PK-PK}
Minimum voltage swing	0.5 V_{PK-PK}
Rise/fall time (20% to 80%)	<500 ps
Undershoot/overshoot	<15%
Output impedance	50 Ohms, nominal
Timing	
Timing resolution	20 ps nominal
Edge accuracy	
Alignment to HSD	
D1 to HSD	±350 ps or ±500 ps, depending on system dash number
Duty cycle	
D1 to D2 accuracy	±150 ps
Programming range	40% to 60%
Edge jitter	10 ps rms typical

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Super Speed Serial Pins (SSSP)

Feature	Specification
Simultaneous drive and receive on a single channel card	
Dual edge strobe mode to detect invalid data	
Internal connections to Superclock (required)	
Internal direct connections to Time Jitter Digitizer	
Per Pin Parametric Measure Module on each wire of differential pair	
Supports Digital Signal I/O	
Two SSSPs can be multiplexed to one pair of pins for double data rate	
Maximum of eight SSSPs per system	
Driver	
Data rate	100 Mbits/s to 400 Mbits/s
Output configuration	Differential
Output impedance	50 Ohms
Rise/fall time	<500 ps; 20% - 80%
Overshoot/undershoot	<15%
Output voltage	
Range	-2.0 V to +5.0 V
Minimum voltage swing	0.5 V_{PK-PK}
Maximum voltage swing	5.0 V_{PK-PK}, to 200 Mb/s 3.3 V_{PK-PK}, to 400 Mb/s
Data drive format	NRZ
Receiver/Comparator	
Configuration	Differential
Compare strobe type	Edge strobe
Data rate	100 Mbits/s to 400 Mbits/s
Differential inputs voltage levels	5.0 V
Input voltage levels relative to ground	-2.0 V to +5.0 V
Comparator termination	
Programmable voltage level, relative to ground	-2.0 V to +5.0 V
Voltage resolution	1 mV; nominal
Impedance	50 Ohms
Compare formats	cmplo, cmphi, cmppat, cmplog, cmpmask, cmpoff
Edge jitter	
Square wave	10 ps rms
Pseudorandom pattern	40 ps rms

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

AC INSTRUMENTATION

Precision Low Frequence Source (PLFS)

Feature	Specification
Peak output voltage (ac + dc)	±11.0 V_{PK}
Waveform resolution	20 bits
Maximum sample rate	25 MHz
Waveform memory size (standard)	64 K samples
Waveform memory segments (standard)	512
Waveform memory size (optional)	1 M samples
Waveform memory segments (optional)	512
DC baseline range	±11.0 V
DC baseline resolution	17 bits
Output impedance	25 Ohm, < 1 Ohm
Lowpass filters	2 k, 20 k, 100 k, 500 kHz
Waveform integrator sample rate	< 20 MHz
Waveform linearity	±2 ppm
Total harmonic distortion	
50 Hz to 2 kHz	115 dB
50 Hz to 20 kHz	110 dB
50 Hz to 100 kHz	95 dB
500 Hz to 250 kHz	75 dB
250 Hz to 500 kHz	55 dB
Total noise (bandwidth)	
50 Hz to 2 kHz (50 Hz to 20 kHz)	110 dB
50 Hz to 20 kHz (50 Hz to 100 kHz)	95 dB
50 Hz to 100 kHz (50 Hz to 100 kHz)	80 dB
500 Hz to 250 kHz (1 MHz)	60 dB
250 kHz to 500 kHz (1 MHz)	55 dB

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Precision Low Frequency Digitizer (PLFD)

Feature	Specification
Peak input voltage (ac + dc)	±11.0 V_{PK}
Waveform resolution	23 bits
Maximum sample rate	25 MHz
Capture memory size	256 K samples
DC baseline range	±11.0 V
DC baseline resolution	17 bits
Input impedance	> 10 MOhm
Input capacitance	<200 pF
Frequency ranges	2 k, 5 k, 20 k, 100 k, 500 kHz
Digital filters 194 selectable filters	(time domain and frequency domain)
Waveform linearity error	±2.0 ppm
Common mode rejection, amplitude range dependent	
dc to 100 Hz	>105 dB
100 Hz to 1 kHz	>85 dB
1 kHz to 20 kHz	>60 dB
20 kHz to 100 kHz	>50 dB
100 kHz to 500 kHz	>35 dB
Total harmonic distortion	
≤ 400 Hz (2 kHz range)	115 dB
400 Hz to 1 kHz (2 kHz range)	110 dB
50 Hz to 5 kHz (5 kHz range)	105 dB
50 Hz to 20 kHz (20 kHz range)	100 dB
50 Hz to 100 kHz (100 kHz range)	80 dB
50 Hz to 500 kHz (500 kHz range)	60 dB
Total noise (bandwidth)	
50 Hz to 5 kHz (50 Hz to 5 kHz)	105 dB
50 Hz to 20 kHz (50 Hz to 20 kHz)	95 dB
50 Hz to 100 kHz (50 Hz to 100 kHz)	80 dB
500 Hz to 500 kHz (50 Hz to 500 kHz)	60 dB

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Low Frequency AC Source (LFAC100 SRC)

Feature	Specification
Peak output voltage (ac + dc)	±11.0 V_{PK}
Waveform resolution	16 bits
Waveform memory	1 meg
DC baseline range	±11.0 V
DC baseline resolution	17 bits
Waveform amplitude range (dc to 100 kHz)	<10.24 V_{PK}
Waveform amplitude resolution	<1 mdB
Output impedance (dc - 100 kHz)	25 Ohms, <1 Ohm
Waveform linearity error	±30 ppm
Total harmonic distortion	
50 Hz - 2 kHz	85 dB
50 Hz - 20 kHz	85 dB
50 Hz - 100 kHz	75 dB
Total noise (bandwidth)	
50 Hz - 1 MHz	85 dB
50 Hz - 100 kHz	75 dB
50 Hz - 1 MHz	65 dB

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Low Frequency AC Digitizer (LFAC100 DIG)

Feature	Specification
Differential input voltage	±11.0 V_{PK}
DC baseline range	±11.0 V_{PK}
DC baseline resolution	17 bits
Input impedance	>10 MOhm
Capture memory depth	256 K samples
Total harmonic distortion	
50 Hz - 20 kHz	85 dB
50 Hz - 100 kHz	75 dB
Total noise (bandwidth)	
50 Hz - 20 kHz	85 dB
50 Hz - 100 kHz	75 dB

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

VHF Measurement Module (VHFMM)

Feature	Specification
Modes	Down-converter, Sampler
Measurement frequency range	5 MHz to 250 MHz
Measurement frequency resolution	1 Hz
Input signal	
Down-converter mode	
Input amplitude	+10 dBm to -75 dBm +10 dBm to -90 dBm, typical
Relative amplitude accuracy	±(0.2 dB + 0.05 dB/dB change)
Sampler mode	See High Frequency Sampler specifications.
Input impedance	50 Ohms nominal
Input VSWR	<2:1, typical
Spectrum	
2nd Order intercept	+50 dBm +60 dBm, typical
3rd Order intercept	+23 dBm +30 dBm, typical
LO-IF leakage	<-70 dBm
LO-RF leakage	<-34 dBm
Image rejection	0 dB
IF Output	
IF nominal center frequency	500 kHz
IF passband	100 kHz to 900 kHz
IF flatness	
100 kHz to 900 kHz	<±1.2 dB
400 kHz to 600 kHz	<±0.75 dB
IF distortion	<-42 dBc
IF spurious	
for input signals < 2.0 dBm	<-50 dBm
for input signals > 2.0 dBm	<-56 dBc

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

VHF Arbitrary Waveform Generator (VHFAWG)

Feature	Specification
Peak output voltage (ac + dc)	±2.0 V_{PK} into 50 Ohm Load
Waveform resolution	12 bits
Maximum sample rate	200 MHz
Waveform memory size	256 K samples 1 M samples optional
Waveform memory segments	4,096
DC baseline range	±2.0 V into 50 Ohms
DC baseline resolution	12 bits
Output impedance	50 Ohm
Lowpass filters	0.5 M, 1.0 M, 2 M, 4 M, 5.5 M, 6 M, 10 M, 15 M, 20 M, 30 M, 45 M, 65 M, 80 MHz
Slew rate (filter bypass)	2000 V/µs typical
Step response filter characteristics	
Risetime	
6 MHz filter	< 70 ns, typical
30 MHz filter	< 22 ns, typical
45 MHz filter	< 18 ns, typical
65 MHz filter	< 9.5 ns, typical
80 MHz filter	< 8 ns, typical
Overshoot/undershoot	
6 MHz filter	< 2%, typical
30 MHz filter	< 2%, typical
45 MHz filter	< 2%, typical
65 MHz filter	< 8%, typical
80 MHz filter	< 8%, typical
Sinewave amplitude absolute accuracy	
dc to 200 MHz	±0.25 dB @ 10 dBm
2nd & 3rd harmonic components	
dc to 4 MHz	–60 dBc
dc to 10 MHz	–55 dBc
dc to 30 MHz	–45 dBc
dc to 200 MHz	–40 dBc
Noise density (bandwidth)	
dc to 80 MHz (100 Hz to 200 MHz)	< 20 µVrms (30 kHz BW)
80 MHz to 200 MHz (100 Hz to 500 MHz)	< 65 µVrms (300 kHz BW)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

VHF Continuous Waveform Source (VHFCW)

Feature	Specification
Peak output voltage (ac + dc)	±2.0 V_{PK} into 50 Ohm Load
DC baseline range	±2.0 V into 50 Ohm Load
DC baseline resolution	12 bits
Output impedance	50 Ohm
Frequency range	1 M to 250 MHz
Frequency resolution	1 Hz
AC amplitude level range	+16 to –31 dBm
AC amplitude level accuracy	±0.25 dB @ +10 dBm
2nd - 5th harmonic components	–70 dBc (1 to 185 MHz)
Non-harmonic spurious	–70 dBc (1 to 185 MHz) –60 dBc (185 to 250 MHz)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Frequency Digitizer (HFD)

Feature	Specification
Peak input voltage (ac + dc)	±20.0 V_{PK}
Waveform resolution	12 bits
Maximum sample rate	20 MHz
Capture memory size	1 M samples
DC baseline range	±12.288 V
DC baseline resolution	12 bits
Input impedance	50 Ohm, 10 kOhm
Lowpass filters	400 k, 2 M, 3.6 M, 6.1 M, 10.0 MHz
Highpass filter	256 kHz
Differential phase (NTSC)	+ 0.5 degrees
Differential gain (NTSC)	+ 0.5%
Sinewave amplitude accuracy	
100 Hz to 1 MHz	±0.3 dB
1 MHz to 5 MHz	±0.5 dB
5 MHz to 9.5 MHz	±1.0 dB
2nd & 3rd harmonic components	
100 Hz to 1 MHz	–60 dB
1 MHz to 5 MHz	–50 dB
5 MHz to 9.5 MHz	–45 dB
Noise density (bandwidth)	
100 Hz to 1 MHz (100 Hz to 5 MHz)	77 dB (30 kHz BW)
1 MHz to 5 MHz (100 Hz to 10 MHz)	77 dB (30 kHz BW)
5 MHz to 9.5 MHz (100 Hz to 10 MHz)	74 dB (30 kHz BW)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Speed Sampler (HSS)

Feature	Specification
Peak input voltage (ac + dc)	±2.048 V_{PK}
Waveform resolution	2 - 16 bits programmable
Maximum effective sample rate	100 GHz
Capture memory size (T_mem)	256 K samples
Capture memory size (DSI/O)	1 M samples
Input bandwidth	dc to 1 GHz
Input impedance (selectable)	37.5, 50, 75, > 10 kOhm
Input capacitance	< 5 pF
Settling time to ±1.5 mV of final value	< 4 ns
Total noise (dc to 1 GHz)	< 100 µVrms
Total harmonic distortion	
dc to 15 MHz	–52 dB typical
dc to 40 MHz	–47 dB typical
dc to 100 MHz	–45 dB typical
Sweep window range	40 ns to 4 µs
Strobe repetition rate	1.3 µs

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Advanced Time Measurement Subsystem (ATMS)

Feature	Specification
Timer/Counter	
Time measurements	
Range	No inherent limits
Resolution	<8 ps
Accuracy	< 1 ns typical
Time base error	2 ppm max. over 1 year operation
Event count	
Range	No limit
Resolution	1 count
Accuracy	±1 count
Maximum count rate	100 MHz
Input selection	digital channels, analog channels, dc channels, TMS channels, trigger bus
Multiple measurement memory	
Range	2 to 1024 measurements
Minimum cycle time	
High resolution	<20 µs
High speed	<400 ns
Measurement modes	Period, frequency, duty cycle, risetime, pulsewidth propagation delay, event count, ratio count, time interval
Start/Stop enable system	
Pre/post counters	
Range	0 to 16,777,215 counts
Resolution	1 count
Accuracy	±0 counts
Maximum Count Rate	100 MHz
Pre/post timers	
Range	0 to 134 ms
Resolution	8 ns
Accuracy	±10 ns
Analog Inputs (TMS and THADS)	
Input capacitance	< 150 pF (TMS channel)
Threshold specifications	
±6 V input range	
Maximum operation	±6.4 V
Threshold resolution	760 µV nominal
Input amplifier noise (En)	<4.0 mV rms
Hysteresis Accuracy	±(20% + 3 mV)
±30 V input range (1 Meg input only)	
Maximum operation	±32.0 V
Threshold resolution	3.8 mV
Hysteresis Accuracy	±(20% + 15 mV)

Advanced Time Measurement Subsystem (ATMS) (continued)

Feature	Specification
Analog Inputs (TMS and THADS) (continued)	
±200 V input range (1 Meg input only)	
Maximum operation	±220.0 V
Threshold resolution	38 mV
Hysteresis Accuracy	±(20% + 150 mV)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Time Jitter Digitizer (TJD)

Feature	Specification
Input channels	3 - analog 2 - SSSP
Independent event selectors	
A event	from ch1, ch3, SSSP1 or SSSP2
B event	from ch1, ch3, SSSP1 or SSSP2
E event	from ch1, ch2, ch3, SSSP1 or SSSP2
Independent time-stampers with independent event enabling	
Automatic	enable after CPU ARM
After A	enable TSb to stamp an event after TSa has stamped an event
After E	enable TSa or TSb after an E event
External	enable TJD after external enable signal
Synchronous	
A event	enable TSa after a TSa input event
B event	enable TSb after a TSb input event
Independent	TSa and TSb stamp continuously and independently
Capture range	0 to 512 ns
Timing resolution	7.8 ps
Time stamp jitter	<10 ps rms
Jitter plus linearity	< 30 ps rms
Time stamp accuracy	1 ppm
Frequency measurement	>350 MHz
Time stamp memory depth	16 k values per time stamper
Capture rate	27.8 MHz
Analog front-end	
Range	±10 V, ±2.5 V
Resolution	1.22 mV

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

MICROWAVE CONTINUOUS WAVEFORM SOURCE

Feature	Specification
Frequency range	4.5 M to 4000 MHz
Frequency resolution	
4.5 MHz to 500 MHz	1 Hz
500 MHz to 1000 MHz	2 Hz
1000 MHz to 2000 MHz	4 Hz
2000 MHz to 4000 MHz	8 Hz
Output impedance	50 Ohm
Level range	+13 to –50 dBm
Level accuracy	
absolute @ +10 dBm	±0.35 dB (4.5 to 50 MHz) ±0.25 dB (50 to 1300 MHz) ±0.35 dB (1300 M to 3000 MHz) ±0.45 dB (3000 M to 4000 MHz)
Level settling time	< 2 ms to 0.02 dB
Frequency settling time	< 500 µs to 0.1 rad
Modulation modes	CW, AM, FM, Phase, Pulse, 0.3 GMSK, Pi/4DQPSK, Arbitrary (with optional IF Modulated Source capability)
Frequency range w/modulation:	5 MHz to 180 MHz (with optional IF Modulated Source capability)
SSB phase noise (@ offset from carrier)	
>-30 dBm output level	
4.5 MHz to 1000 MHz	-104 dBc @ 1 kHz -114 dBc @ 10 kHz -120 dBc @ 10 MHz
1000 MHz to 2000 MHz	-98 dBc @ 1 kHz -118 dBc @ 10 kHz -114 dBc @ 10 MHz
2000 MHz to 4000 MHz	-92 dBc @ 1 kHz -102 dBc @ 10 kHz -108 dBc @ 10 MHz
SSB phase noise (@ offset from carrier)	
-30 dBm to -50 dBm output level	
4.5 MHz to 1000 MHz	-103 dBc @ 1 kHz -107 dBc @ 10 kHz -108 dBc @ 10 MHz
1000 MHz to 2000 MHz	-98 dBc @ 1 kHz -105 dBc @ 10 kHz -108 dBc @ 10 MHz
2000 MHz to 4000 MHz	-92 dBc @ 1 kHz -102 dBc @ 10 kHz -108 dBc @ 10 MHz

MICROWAVE CONTINUOUS WAVEFORM SOURCE (CONTINUED)

Feature	Specification
Harmonic Spurious (@ output power level)	
4.5 MHz to 1000 MHz	-27 dBc @ 12-13 dBm
	-27 dBc @ 11-12 dBm
	-29 dBc @ 10-11 dBm
	-29 dBc @ 5-10 dBm
	-29 dBc @ 0-5 dBm
	-30 dBc @ <0 dBm
1000 MHz to 2000 MHz	-25 dBc @ 12-13 dBm
	-27 dBc @ 11-12 dBm
	-28 dBc @ 10-11 dBm
	-29 dBc @ 5-10 dBm
	-32 dBc @ 0-5 dBm
	-35 dBc @ <0 dBm
2000 MHz to 4000 MHz	-30 dBc @ 12-13 dBm
	-31 dBc @ 11-12 dBm
	-32 dBc @ 10-11 dBm
	-33 dBc @ 5-10 dBm
	-35 dBc @ 0-5 dBm
	-35 dBc @ <0 dBm
Non-harmonic spurious	
4.5 MHz to 1000 MHz	-54 dBc
1000 MHz to 2000 MHz	-50 dBc
2000 MHz to 4000 MHz	-46 dBc
Residual FM (in 300 Hz to 15 kHz BW)	
4.5 MHz to 1000 MHz	<7 Hz
1000 MHz to 2000 MHz	<13 Hz
2000 MHz to 4000 MHz	<25 Hz
Output VSWR	
4.5 MHz to 1000 MHz	<1.5:1 output, typical
1000 MHz to 2000 MHz	<1.7:1 output, typical
2000 MHz to 3000 MHz	<2.0:1 output, typical
3000 MHz to 4000 MHz	<2.2:1 output, typical

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

DC INSTRUMENTATION

DC Subsystem (V/I): 60 V/200 mA V/I Sources

Feature	Specification
Voltage forcing accuracy (16-bit resolution; nominal)	
±200 V range	±(0.1% or 100 mV); 6.250 mV resolution
100 V range	±(0.1% or 50 mV); 3.125 mV resolution
50 V range	±(0.05% or 25 mV); 1.563 mV resolution
20 V range	±(0.05% or 5 mV); 625.0 µV resolution
10 V range	±(0.05% or 2.5 mV); 312.50 µV resolution
5 V range	±(0.05% or 1.0 mV); 156.25 µV resolution
2 V range	±(0.05% or 1.0 mV); 62.50 µV resolution
1 V range	±1.0 mV; 31.25 µV resolution
0.5 V range	±1.0 mV; 15.63 µV resolution
Voltage measuring accuracy (14-bit resolution; nominal)	
±200 V range	±(0.1% or 100 mV); 25 mV resolution
100 V range	±(0.1% or 50 mV); 12.50 mV resolution
50 V range	±(0.05% or 25 mV); 6.25 mV resolution
20 V range	±(0.05% or 5 mV); 3.125 mV resolution
10 V range	±(0.05% or 2.5 mV); 1.563 mV resolution
5 V range	±(0.05% or 1.0 mV); 625.0 µV resolution
2 V range	±(0.05% or 1.0 mV); 312.50 µV resolution
1 V range	±1.0 mV; 156.25 µV resolution
0.5 V range	±1.0 mV; 62.50 µV resolution
Current forcing accuracy (12-bit resolution; nominal)	
±200 mA range	±(0.1% + 200 µA); 100 µA resolution
20 mA range	±(0.1% + 20.0 µA); 10.0 µA resolution
2 mA range	±(0.1% + 2.0 µA); 1.0 µA resolution

DC Subsystem (V/I): 60 V/200 mA V/I Sources (continued)

Feature	Specification
Current forcing accuracy (12-bit resolution; nominal) (continued)	
200 µA range	±(0.1% + 300 nA + 1 nA/V); 100 nA resolution
20 µA range	±(0.1% + 120 nA + 1 nA/V); 10 nA resolution
Current measurinting accuracy (14-bit resolution; nominal)	
±200 mA	±(0.1% + 100 µA) 25 µA resolution
100 mA	±(0.1% + 50 µA) 12.50 µA resolution
50 mA	±(0.1% + 25 µA) 6.25 µA resolution
20 mA	±(0.1% + 10 µA) 2.50 µA resolution
10 mA	±(0.1% +5 µA) 1.25 µA resolution
5 mA	±(0.1% + 2.5 µA) 625 nA resolution
2 mA	±(0.1% + 1 µA) 250 nA resolution
1 mA	±(0.1 % + 600 nA + 1 nA/V) 125 nA resolution
500 µA	±(0.1% + 350 nA + 1 nA/V) 62.50 nA resolution
200 µA	±(0.1 % + 200 nA + 1 nA/V) 25 nA resolution
100 µA	±0.1% + 150 nA + 1 nA/V) 12.50 nA resolution
50 µA	±(0.1% + 125 nA + 1 nA/V) 6.25 nA resolution
20 µA	±(0.1 % + 110 nA + 1 nA/V) 2.50 nA resolution
10 µA	±(0.1% + 105 nA + 1 nA/V) 1.25 nA resolution
5 µA	±(0.1% + 103 nA + 1 nA/V) 625 pA resolution

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

DC Subsystem: DC Differential Voltmeter

Feature	Specification
Voltage metering accuracy (14-bit resolution; nominal)	
±200 V range	±(0.1% or 100 mV); 25 mV resolution
100 V range	±(0.1% or 50 mV); 12.50 mV resolution
50 V range	±(0.05% or 25 mV); 6.25 mV resolution
20 V range	±(0.05% or 5 mV); 3.125 mV resolution
10 V range	±(0.05% or 2.5 mV); 1.563 mV resolution
5 V range	±(0.05% or 1.0 mV);
1 V range	±1.0 mV; 156.25 µV resolution
0.5 V range	±1.0 mV; 62.50 µV resolution
Common mode rejection ratio	80 dB @ dc
Maximum allowable voltage	±65 V dc to ground
Sample and difference	
Gain	x1, x10, xl00 measured range
Accuracy	
Xl, X10	±(0.5% + 0.1% F.S.)
X100	±(l.0% + 1.0% F.S.)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Analog Pin Unit (APU)

Feature	Specification
APU per-pin architecture	
Number of pins	48 pins maximum 2 head multiplex
Matrix access	8 lines per APU
Controller	MC68000 microprocessor per group of 24 APUs
Memory per 24 pins	4,096 locations x 12 bits
APU functions/modes	
Functions/modes	Force V, Measure I Force I, Measure V
Maximum operating voltage	±24 V
Maximum operating current	±30 mA
Voltage forcing accuracy (12-bit resolution; nominal)	
2 V range	±(0.1% + 1.5 mV); 1.00 mV resolution
5 V range	±(0.1% + 3.7 mV); 2.50 mV resolution
10 V range	±(0.1% + 7.5 mV); 5.00 mV resolution
24 V range	±(0.1% + 18 mV); 12.00 mV resolution
Voltage measuring	
System A/D converter accuracy (14-bit resolution; nominal)	
2 V range	±(0.1% + 1.2 mV); 250 μV resolution
5 V range	±(0.1% + 3.0 mV); 625 μV resolution
10 V range	±(0.1% + 6.0 mV); 1.25 mV resolution
24 V range	±(0.1% + 14.4 mV); 3.00 mV resolution
Voltage measuring	
Local A/D converter accuracy (12-bit resolution; nominal)	
2 V range	±(0.1% + 2.8 mV); 1.00 mV resolution
5 V range	±(0.1% + 6.3 mV); 2.50 mV resolution
10 V range	±(0.1% + 12.5 mV); 5.00 mV resolution
24 V range	±(0.1% + 30.0 mV); 12.00 mV resolution

Analog Pin Unit (APU) (continued)

Feature	Specification
Current forcing accuracy (12-bit resolution; nominal)	
200 µA range	±(0.1% + 0.3 µA + 2 nA/V); 100 nA resolution
1 mA range	±(0.1% + 1.1 µA); 500 nA resolution
5 mA range	±(0.1% + 5.0 µA); 2.50 µA resolution
30 mA range	±(0.1% + 30.0 µA); 15.0 µA resolution
Current measuring	
System A/D converter accuracy (14-bit resolution; nominal)	
2 µA range	±(0.5% + 110 nA + 1 nA/V); 0.25 nA resolution
10 µA range	±(0.2% + 110 nA + 1 nA/V); 1.25 nA resolution
50 µA range	±(0.2% + 300 nA + 1 nA/V); 6.25 nA resolution
200 µA range	±(0.1% + 0.25 µA + 2 nA/V); 25 nA resolution
1 mA range	±(0.1% + 0.85 µA); 125 nA resolution
5 mA range	±(0.1% + 3.7 µA); 625 nA resolution
30 mA range	±(0.1% + 22.5 µA); 3.75 µA resolution
Local A/D converter accuracy (12-bit resolution; nominal)	
2 µA range	±(0.5% + 110 nA + 1 nA/V); 1.0 nA resolution
10 µA range	±(0.2% + 115 nA + 1 nA/V); 5.0 nA resolution
50 µA range	±(0.2% + 300 nA + 1 nA/V); 25 nA resolution
200 µA range	±(0.1% + 0.4 µA + 2 nA/V); 100 nA resolution
1 mA range	±(0.1% + 1.6 µA); 0.5 µA resolution
5 mA range	±(0.1% + 7.5µA); 2.5 µA resolution
30 mA range	±(0.1% + 45 µA); 15 µA resolution

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Advanced Analog Pin Unit (AAPU)

Feature	Specification
AAPU per-pin architecture	
Number of pins	68 pins maximum 2 head multiplex
Matrix access	8 lines per AAPU
Controller	Custom gate array controller per group of 4 AAPUs
AAPU voltage measure mode (high-Z)	Force V, Measure I Force I, Measure V
Maximum operating voltage	±30 V
Maximum operating current	±30 mA
Programmable current clamp (Force V mode)	±30 mA
Programmable voltage clamp (Force I mode)	±30 V
Voltage forcing accuracy (14-bit resolution; nominal)	
2 V range	±(0.1% + 1.5 mV); 0.25 mV resolution
5 V range	±(0.1% + 3.0 mV); 0.625 mV resolution
10 V range	±(0.1% + 6.0 mV); 1.25 mV resolution
30 V range	±(0.1% + 18 mV); 3.75 mV resolution
Voltage measuring	
System A/D converter accuracy (14-bit resolution; nominal)	
2 V range	±(0.1% + 1.5 mV); 0.25 mV resolution
5 V range	±(0.1% + 3.0 mV); 0.625 mV resolution
10 V range	±(0.1% + 6.0 mV); 1.25 mV resolution
30 V range	±(0.1% + 18.0 mV); 3.75 mV resolution
Current forcing accuracy (14-bit resolution; nominal)	
200 µA range	±(0.1% + 0.25 µA + 1 nA/V); 25 nA resolution
1 mA range	±(0.1% + 0.8 µA); 0.125 nA resolution
5 mA range	±(0.1% + 4.0 µA); 0.625 nA resolution
30 mA range	±(0.1% + 24.0 µA); 3.75 nA resolution
Current measuring (14-bit resolution; nominal)	
2 µA range	±(0.5% + 110 nA + 1 nA/V); 0.25 nA resolution
10 µA range	±(0.2% + 120 nA + 1 nA/V); 1.25 nA resolution
50 µA range	±(0.2% + 200 nA + 1 nA/V); 6.25 nA resolution

Advanced Analog Pin Unit (AAPU) (continued)

Feature	Specification
Current measuring (14-bit resolution; nominal)	
200 µA range	±(0.1% + 0.3 µA + 1 nA/V); 25 nA resolution
1 mA range	±(0.1% + 1.0 µA); 125 nA resolution
5 mA range	±(0.1% + 5.0 µA); 625 nA resolution
30 mA range	±(0.1% + 30 µA); 3.75 µA resolution

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Current Unit (HCU)

Feature	Specification
Voltage forcing ±30 V (14-bit resolution)	
2 V range	
Resolution	250 µV
Accuracy	±(0.1% +1.5 mV)
30 V range	
Resolution	3.75 mV
Accuracy	±(0.1% +15 mV)
Current forcing ±2 A (12-bit resolution)	
20 mA range	
Resolution	5 µA
Accuracy	±(0.1% + 20 µA)
200 mA range	
Resolution	50 µA
Accuracy	±(0.1% + 200 µA)
2 A range	
Resolution	500 µA
Accuracy	±(0.2% + 2 mA)
Current measuring ±2 A (14-bit resolution)	
20 mA range	
Resolution	5 µA
Accuracy	±(0.1% + 20 µA)
200 mA range	
Resolution	50 µA
Accuracy	±(0.1% + 200 µA)
2 A range	
Resolution	500 µA
Accuracy	±(0.2% + 2 mA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Quad Power V/I (QPVI)

Feature	Specification
Four independent 50 V/30 A floating supplies that can be serially stacked for higher voltages or operated in parallel for higher currents	
Two-/Four-quadrant operation with voltage polarity switching (I and IV or II and III)	
Modulation support for duty cycle and pulse mode	
Fully floating to ±300 V to ground	
Z_{OUT} = Low for 0 V when gated off, or Z_{OUT} = High for 0 A when gated off	
Voltage forcing	
Ranges	2 V, 10 V, 50 V
Resolution	11 bits plus sign
Voltage metering	
Ranges	2 V, 10 V, 50 V
Resolution	13 bits plus sign
Current forcing	
Ranges	40 mA, 200 mA, 1 A, 5 A, 30 A
Resolution	11 bits plus sign
Current metering	
Ranges	40 mA, 200 mA, 1 A, 5 A, 30 A
Resolution	13 bits plus sign

Quad Op Amp Loop (QOA)

Feature	Specification
Number of parallel Op Amps	4
Selectable loop gain polarity	
Loop gain settings	100, 1000, 10000
VOS measurement Ranges Accuracy Gain of 100 Gain of 1,000 Gain of 10,000	 ±970 nV to ±99 mV 0.25% of setting 0.25% of setting 0.5% of setting
Output load resistors	600, 2 k, 10 kOhm
Oscillation detector threshold	20 mV to 3.32 V, programmable
Commutation	256 time slots driven by one of eight trigger bus lines

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Low Current Ammeter (LCA)

Feature	Specification
Number of parallel measurements	8
Resistive mode accuracy	
10 uA range	±1.5% of reading ±50 nA
1 µA range	±1.5% of reading ±5 nA
100 nA range	± 2.0% of reading ±500 pA
Integrate mode measurement accuracy	
10 nA range (1 power line cycle)	±2.0% of reading ±50 pA
1 nA range (1 power line cycle)	±2.5% of reading ±5 pA + Fixture error
100 pA range (1 power line cycle)	±3.5% of reading ±2 pA + Fixture error
10 pA range (10 power line cycle)	±3.5% of reading ±2 pA + Fixture error

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Pulse Driver

Feature	Specification
Pulse settings	
Delay and width ranges	100 ns, 400 ns, 1.6 µs, 6.4 µs, 25 µs, 100 µs, 400 µs, 1.6 ms, 4 ms
RF output channel performance	
Impedance	50 Ohm
Rise time (10 V swing)	< 15 ns
Settling time @ 1%	< 50 ns
Maximum unloaded swing	±5.5 V
Pogo output channel performance	
Impedance	95 Ohm
Rise time (selectable) (20 V swing)	35 ns, 85 ns
Settling time @ 1% (selectable)	< 100 ns, < 250 ns
Maximum unloaded swing	±11 V

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Precision Multimeter (PMM)

Feature	Specification
DC voltage measurement 1.0 dc Volts; 1.1 accuracy Units are ppm of reading + ppm of range. Specifications are for 100 periodic line cycles.	
100 mV range	2.5 + 85; typical, 24 hours 3.5 + 90; 90 day
1 V range	1.5 + 8.5; typical, 24 hours 3.1 + 9; 90 day
10 V range	0.5 +0.85; typical, 24 hours 2.6 +1; 90 day
100 V range	2.5 + 0.38; typical, 24 hours 4.5 + 0.38; 90 day
DC current measurement 2.0 dc current; 2.1 accuracy Units are ppm of reading + ppm of range, unless otherwise noted. Specifications are for 100 periodic line cycles.	
100 nA range	10 +3; typical, 24 hours 30 + 3; 90 day
1 µA range	10 + 0.3; typical, 24 hours 15 + 0.3; 90 day
10 µA range	10 + 300; typical, 24 hours 15 + 310; 90 day
100 µA range	10 + 35; typical, 24 hours 15 + 38; 90 day
1 mA range	10 + 6; typical, 24 hours 15 + 8; 90 day
10 mA range	10 + 3.3; typical, 24 hours 15 + 5.3; 90 day
100 mA range	25 + 3; typical, 24 hours 30 + 5; 90 day
1 A range	100 + 10; typical, 24 hours 100 + 10; 90 day
Resistance measurement accuracy Units are ppm of reading + ppm of range Specification applies for measurements over 100 periodic line cycles.	
4-Wire mode	
10 Ohm range	6 + 3; typical, 24 hours 16 + 5; 90 day
100 Ohm range	9 + 3; typical, 24 hours 16 +5; 90 day
1 kOhm range	8 + 0.2; typical, 24 hours 14+ 0.5; 90 day
10 kOhm range	62 + 0.2; typical, 24 hours 68 + 0.5; 90 day
100 kOhm range	120 + 0.2; typical, 24 hours 130 + 0.5; 90 day

Precision Multimeter (PMM) (continued)

Feature	Specification
Resistance measurement accuracy Units are ppm of reading + ppm of range Specification applies for measurements over 100 periodic line cycles.	
2-Wire mode	
1 MOhm range	610 + 8; typical, 24 hours 610 + 9; 90 day
10 MOhm range	0.6% + 5.7; typical, 24 hours 0.6% + 11; 90 day
100 MOhm range	0.65% + 10; typical, 24 hours 0.65% + 10; 90 day
1 GOhm range	1.1 % + 10; typical, 24 hours 1.1 % + 10; 90 day

AC voltage measurement accuracy
Units are % of reading + % of range - for inputs 1/20th F.S. rms to F.S. rms

Range	10 - 20 Hz	20 - 40 Hz	40 Hz - 1 kHz	1 - 20 kHz
1 V	0.117 + 0.024	0.041 + 0.01	0.022 + 0.0034	0.029 + 0.0034
10 V	0.117 + 0.024	0.041 + 0.01	0.022 + 0.0034	0.029 + 0.0034
100 V	0.13 + 0.024	0.054 + 0.01	0.036 + 0.004	0.036 + 0.015

Range	20 - 50 kHz	50 - 100 kHz	I00 - 200 kHz	200 - 300 kHz
1 V	0.1 + 0.004	0.5 + 0.01	2 + 0.03	3.5 + 0.05
10 V	0.1 + 0.004	0.5 + 0.006	2 + 0.03	3.5 + 0.06
100V	0.12 + 0.025	0.56 + 0.012	2 + 0.12	3.5 + 0.12

Range	300 - 400 kHz	400 - 500 kHz
1 V	5.5 + 0.05	8.5 + 0.05
10 V	5.5 + 0.06	8.5 + 0.06
100 V	5.5 + 0.12	8.5 + 0.12

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Precision Reference Source

Feature	Specification
Voltage Range	±11.0 V
Voltage Resolution	17 Bits, 168 µV
Noise over 20 kHz Bandwidth	< 20 µVrms
Settling Time to 1 ppm of Final Value	< 2 ms

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

SYNCHRONIZED POWER INSTRUMENTATION

High Current Current Source (HCCS)

Feature	Specification
HCCS functions/modes	
100 A/30 V current source - A current source with programmable voltage clamp	
100 A/100 V current load - A current load with programmable voltage clamp	
Floating for high-side applications	
Force zero volts for short circuit testing	
Independent voltage and current measuring	
Trigger Bus control for gate signal	
Two-station multiplexed via High Power Matrix (HPM)	
Current source mode accuracy (nominal resolution)	
Range	
1 A	±(0.5% + 5 mA) 30.5 µA resolution
5 A	±(0.5% + 12.5 mA) 152.5 µA resolution
10 A	±(0.5% + 25 mA) 305 µA resolution
100 A	±(0.5% + 250 mA) 3.05 mA resolution
Settling time (non-reactive load)	
Compliance Points	
To specification	< 500 µs
at 100 µs	±3% of final value
Current measuring accuracy	
Note: Resolution is that of the instrument used on the Measure Bus, typically system dc voltmeter	
Range	
1 A	±(0.5% + 5 mA)
5 A	±(0.5% + 12.5 mA)
10 A	±(0.5% + 25 mA)
100 A	±(0.5% + 250 mA)

Compliance Points (settling time):

30 V Range	DC	100 ms	1 ms
Source	25 V/15 A	17 V/50 A	14 V/100 A
-30 V Range	DC	100 ms	1 ms
Load	-25 V/15 A	-17 V/50 A	-14 V/100 A

High Current Current Source (HCCS) (continued)

Feature	Specification
Voltage measuring accuracy	
Note: Resolution is that of the instrument used on the Measure Bus, typically system dc voltmeter	
Range	
100 V	±(0.5% + 100 mV)
20 V	±(0.5% + 20 mV)
10 V	±(0.5% + 10 mV)
2 V	±(0.5% + 5 mV)
Voltage Clamping	
Range	
100 V	±(1.5% + 1.0 V) + (1.5 V*(Iactual/Irange)
Resolution	12.5 mV

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Current Voltage Source (HCVS)

Feature				Specification
HCVS functions/modes				
120 V/100 A - A voltage source with programmable current clamp				
Floating for negative supply applications				
Automatic crossover to power sinking quadrant for capacitive discharge				
Independent voltage and current measuring				
Trigger Bus control for gate signal				
Two-station multiplexed via High Power Matrix (HPM)				
Compliance (<10% duty cycle)				
V Range	DC	10 ms	1 ms	
30 V	25 V/12 A	15 V/50 A	12 V/100 A	
60 V	50 V/6 A	40 V/40 A	45V/65 A	
90 V	80 V/3 A	70 V/20 A	75 V/40 A	
120 V	110 V/2 A	100 V/12 A	110 V/25 A	
Voltage forcing accuracy				
Range				
30, 60, 90, 120 V				±(0.5% + 150 mV)
Resolution				1.83 mV (nominal)
Settling time (non-reactive load)				
To specification				< 500 µs
at 100 µs				±3% of final value
Voltage measuring accuracy				
Range				
150 V				±(0.5% + 150 mV)
Current measuring accuracy				
Range				
100 A				±(1.0% + 250 mA)
10 A				±(1.0% + 25 mA)
1 A				±(1.0% + 5 mA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Power V/I (HPVI)

Feature	Specification
High Power V/I Functions/Modes	
750 V/10 A - A voltage source with programmable current clamp	
750 V/10 A - A current source with programmable voltage clamp	
Floating for negative supply applications	
Automatic crossover to power sinking quadrant for capacitive discharge	
Independent voltage and current measuring	
Trigger Bus control for gate signal	
Two-station multiplexed via High Power Matrix (HPM)	

Compliance points (<10% duty cycle. 40% F.S. <VOUT <F.S.)

VRange	DC	100 ms	10 ms	1 ms
85 V	4.0 A	8.0 A	10.0 A	10.0 A
170 V	2.0 A	5.0 A	7.0 A	10.0 A
225 V	1.4 A	4.0 A	4.5 A	8.5 A
340 V	1.0 A	3.5 A	4.0 A	7.0 A
510 V	700 mA	2.0 A	2.2 A	4.2 A
750 V	500 mA	1.9 A	2.0 A	3.5 A

Feature	Specification
Voltage forcing accuracy	
Range	
85 V	±(0.5% + 250 mV) 6.25 mV resolution
170 V	±(0.5% + 250 mV) 6.25 mV resolution
255 V	±(0.5% + 500 mV) 12.5 mV resolution
340 V	±(0.5% + 500 mV) 12.5 mV resolution
510 V	±(1.0% + 1.0 V) 12.5 mV resolution
750 V	±(1.0% + 1.0 V) 12.5 mV resolution
Voltage forcing settling time (non-reactive load)	
To specification	<500 µs
at 100 µs	±3% of final value
Voltage measuring accuracy	
Range	
800 V	±(0.5% + 1.0 V)

High Power V/I (HPVI) (continued)

Feature	Specification
Current forcing accuracy	
Range; V Range	
100 mA; 510 V, 750 V	±(l.5% + 1 mA) 25 µA resolution
100 mA; 85– 340 V	±(l.5% + 2 mA) 50 µA resolution
10 A; 510 V, 750 V	±(l.5% + 25 mA) 2.5 mA resolution
10 A; 85 –340 V	±(3.0% + 50 mA) 5 mA resolution
Current forcing settling time (non-reactive load)	
To specification	< 1 ms
at 100 µs	±3% of final value
Current measuring accuracy	
Range	
10 A	±(l.0% + 12.5 mA)
1 A	±(l.0% + 8.5 mA)
100 mA	±(l.0% + 125 µA)
10 mA	±(l.0% + 85 µA)
1 mA	±(1.5% + 2 .0 µA)
100 µA	±(1.5% +2.0 µA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Power Matrix (HPM)

Feature	Specification
HPM Functions/Modes	
Four lines (two instruments) by 12 pins	
Two high current lines (10 A per pin)	
Two medium current lines (5 A per pin)	
1,000 V operating voltage	
Guarded Kelvin connections (force, sense, guard)	
Parallel pins for currents up to 80 A pulsed	
Per-pin access to low power matrix for dc parametrics	
Crowbar protection for dc matrix connections	
Separate series and parallel access for HV Ammeter	
Up to 2 HPMs (24 hp pins) per SP card cage	
Two-station multiplexed	
High Current Lines (1 & 2)	
Pulsed current is defined as <10 ms and <10% duty cycle	
Maximum current per pin, dc, not switched	10 A
Maximum current per pin, switched	1 A
Maximum current per pin, pulsed	20 A
Maximum current per line, dc	40 A
Maximum current per line, pulsed	80 A
Medium Current Lines (3 & 4)	
Pulsed current is defined as <10 ms and <10% duty cycle	
Maximum current per pin, dc, not switched	5 A
Maximum current per pin, switched	1 A
Maximum current per pin, pulsed	10 A
Maximum current per line, dc	20 A
Maximum current per line, pulsed	40 A
Maximum Voltage	
All nodes, non switching	1,000 V
DC Matrix Interface	
Maximum current	1 A
Maximum voltage (crowbar off)	±200 V (nominal)
Maximum voltage (crowbar on)	±60 V (nominal)
Maximum leakage (crowbar off)	±1 µA (typical)
Maximum leakage (crowbar on)	±10 µA (typical)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

High Voltage Ammeter (HVA)

Feature	Specification
HVA Functions/Modes	
1 µA to 100 mA current ranges	
Floating 1,400 V for high-side measurements (pin to pin)	
High Power Matrix output	
Two-station multiplexed	
HVA Connections	
HP Matrix connections	In series with line 4; In parallel with lines 1 & 2
Current Measuring Accuracy (14 bits nominal)	
Note: Resolution is that of the instrument used on the Measure Bus, typically system dc voltmeter	
Range	
100 mA	±(0.2% + 120 µA)
10 mA	±(0.2% + 12 uA)
1 mA	±(0.2% + 1.2 µA)
100 µA	±(0.2% + 120 nA)
10 µA	±(0.2% + 30 nA)
1 µA	±(0.5% + 20 nA)

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

Breakdown Voltage Current Source (BVCS)

Feature	Specification
Forcing current source accuracy	
Range	
10 µA	±(0.5% + 50 nA) 305 pA resolution (nominal)
100 µA	±(0.5% + 500 nA) 3.05 nA resolution (nominal)
1 mA	±(0.5% + 5 µA) 30.5 nA resolution (nominal)
10 mA	±(0.5% + 50 µA) 305 nA resolution (nominal)
Maximum programmable output current	
BVCS as current source	10 mA
Maximum programmable output voltage	
High power V/I as voltage supply	750 V
High voltage source as voltage supply	800 V
Voltage measurement accuracy	
Range	
50 V	±0.5% + 0.50 V)
200 V	±(0.5% + 1.00 V)
1000 V	±0.5% + 1.25 V)
Output resistance (Rout)	
Irange = 10 mA	249.7 Ohms
Irange = 1 mA	453.5 Ohms
Irange = 100 µA	493.8 Ohms
Irange = 10 µA	498.3 Ohms
Irange = 1 µA	498.8 Ohms
Maximum programmable output voltage	
High power V/I as voltage supply	750 V
Maximum programmable output current	10 mA
Current measurement accuracy (% of reading + offset)	
Range	
1 µA	±(0.5% + 10 nA)
10 µA	±(0.5% + 50 nA)
100 µA	±(0.5% + 500 nA)
1 mA	±(0.5% + 5 µA)
10 mA	±(0.5% + 50 µA)
Ammeter settling time	<100 µs typical
Maximum allowable current	10 mA

These specifications are subject to change. Please contact your Teradyne sales engineer for current specifications. Some specifications will vary based on the test head used.

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