Flexible Circuit Design Guide

Fourth Edition

TELEDYNE
ELECTRONIC TECHNOLOGIES
A Teledyne Technologies Company

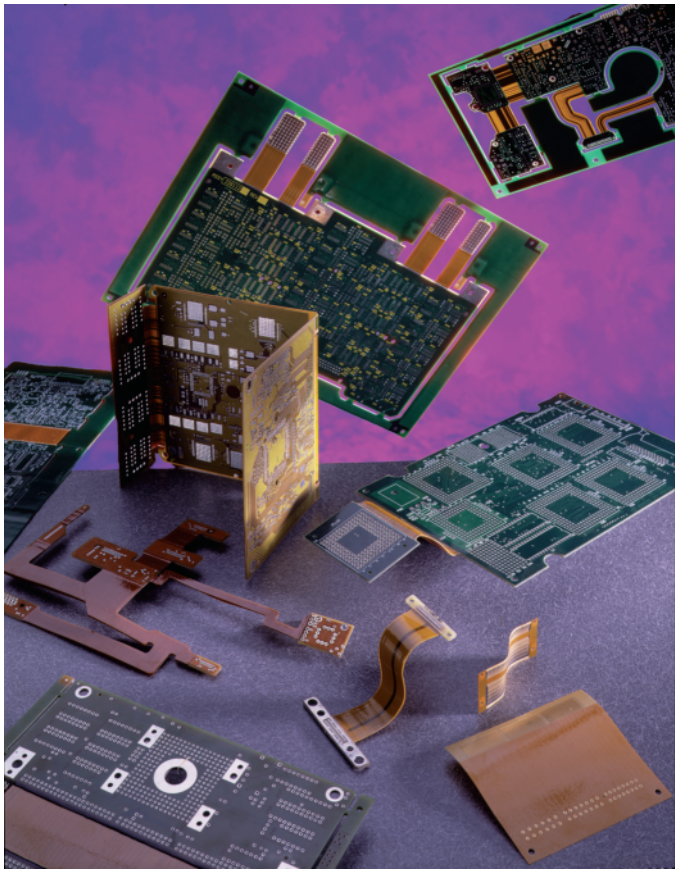
Teledyne Electronic Technologies
Leading the interconnection field since 1963.

Teledyne Electronic Technologies (TET), formerly Teledyne Electro-Mechanisms, has been a leader in the field of interconnection technology since its incorporation in 1963. At that time we designed and manufactured innovative single layer flexible circuits and unique multilayer rigid-flex harnesses to support the NASA Saturn V program.

Throughout the years our design engineers and manufacturing personnel have worked together perfecting solutions to customer design challenges from the simplest single layer applications to the most complex interconnection systems. TET is proud to hold numerous process patents related to flexible circuit manufacturing.

Today we continue to be in the forefront of the industry by contributing to a multitude of military and commercial applications. In addition to the standard circuits we have produced for many years, TET is continuing to develop new and better products in the flexible circuit and multilayer rigid-flex marketplace.

Teledyne is committed to assisting our customers from design development right through prototypes and production. This commitment includes a fully staffed engineering department utilizing the latest CAD/CAM/CIM systems for circuit design, document creation, artwork generation, and drill/rout program creation. Our product engineers specialize in optimizing available tooling systems to help control costs.



TELEDYNE ELECTRONIC TECHNOLOGIES

Printed Circuit Technology Business Unit

110 Lowell Road, CS 68

Hudson, New Hampshire 03051

Tel: (603) 889-6191

Fax: (603) 882-4457

Email: sales@tetpct.com

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Design Guide Purpose and Use

Purpose of this Design Guide — Designing for Manufacture

This Design Guide is provided to assist you in designing the most cost-effective flexible circuits for your electronic packaging needs. It is our belief that designers who are aware of the processes used in the manufacture of flexible printed circuits will be rewarded by a circuit design that will effectively make use of all the advantages that these types of electronic interconnects have to offer.

This Design Guide is meant to be a reference for the electrical, mechanical, and artwork considerations which must be addressed when designing a flexible circuit. As needed, the materials and processes used in their manufacture are described in detail so that informed tradeoffs and design decisions can be made. By following the guidelines presented here, your design will be both cost-effective and producible. When used as a design reference, this Design Guide is not meant to override any existing military specifications or commercial preferred design practices, but supports them both. The information contained herein is based on Teledyne Electronic Technologies' extensive experience as a designer and manufacturer of quality flexible and rigid-flex circuitry.

As you prepare to embark on a flexible circuit design program, Teledyne Electronic Technologies' design and engineering staff is on call to assist you. Please contact us with any questions regarding your electronic packaging needs.

What the designer needs to know

There are many parameters that must be determined before beginning an electromechanical design incorporating flexible or multi-layer flexible circuitry. The designer must fully understand the electrical properties of the system, such as current maximums, voltages, types of signals (video, digital, RF, etc.), shielding considerations, impedance characteristics, and capacitance limitations. It is essential to define the circuit components selected, including connectors. To assist the manufacturer, the location of all components should be included. Also necessary is a detailed wire listing, net list and schematic. To allow the manufacturer the greatest amount of flexibility, only terminal areas, rather than specific pin-to-pin conductor runs, should be specified. This provides the manufacturer the necessary freedom to keep the circuit crossover points to a minimum, and reduce the total number of circuit layers necessary.

Please refer to the section of this guide titled *Electrical Design* for assistance in meeting the electrical concerns of your design. If you choose to have Teledyne's experienced staff of electromechanical designers provide a finished design, it will be necessary to provide the electrical parameters listed above to assure an electrically sound design.

After the electrical parameters are defined, the overall physical requirements of the system must be determined. As a minimum, the designer should be provided with dimensioned prints of the unit and appropriate cross-sectional views. Dimensioned prints should be clear and detailed to avoid costly tooling errors. On all prototype designs for fit evaluation only, Teledyne's product engineers will minimize tooling costs by taking the necessary steps.

The design of a flexible circuit interconnection system is facilitated by using an actual unit or an accurate mock-up, or by using three dimensional software programs such as AutoCad or Pro-E™, rather than relying solely on dimensioned prints. By using a box, a series of Mylar or paper "dolls" can be made to determine mechanical

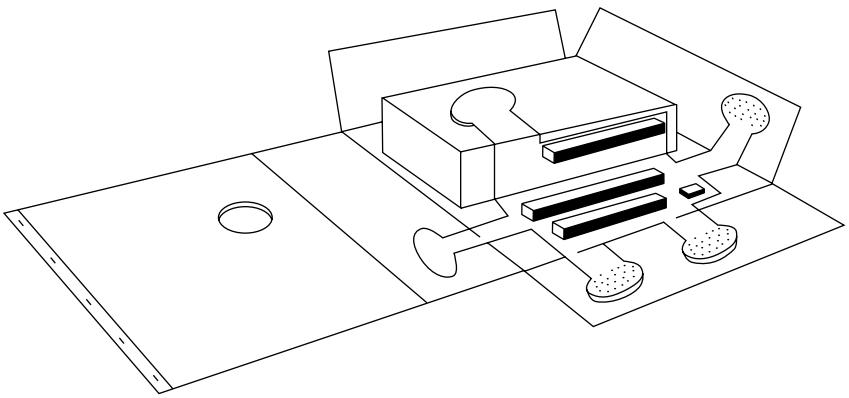


Figure 1-1. "Mylar doll" cutout

approaches and general configurations. The unit or mock-up should have all the required hardware installed to make the design complete and prevent physical interference. Refer to Figure 1-1. The flex harness must be designed to fit the general assembly sequence of its unit, so the cables do not cover any components that may require service or replacement. Cables should not be routed over an area where a component must be installed after the assembly is completed. If the flexible section of the unit will be designed to flex when the box is opened, then an adequate "service loop" should be incorporated in the design. This service loop should be long enough to allow access to the inside of the unit but should not interfere with any other components when installed. Refer to Figure 1-2.

The final consideration is the environmental conditions to which the system will be subjected. Thermal rises, atmospheric conditions, humidity, vibration, and handling are all environmental factors that can influence design criteria. Adequate strain relief and sealing must be provided for moisture and vibration applications. If the unit is subjected to constant thermal cycling, special consideration must be used when choosing insulating and bonding materials.

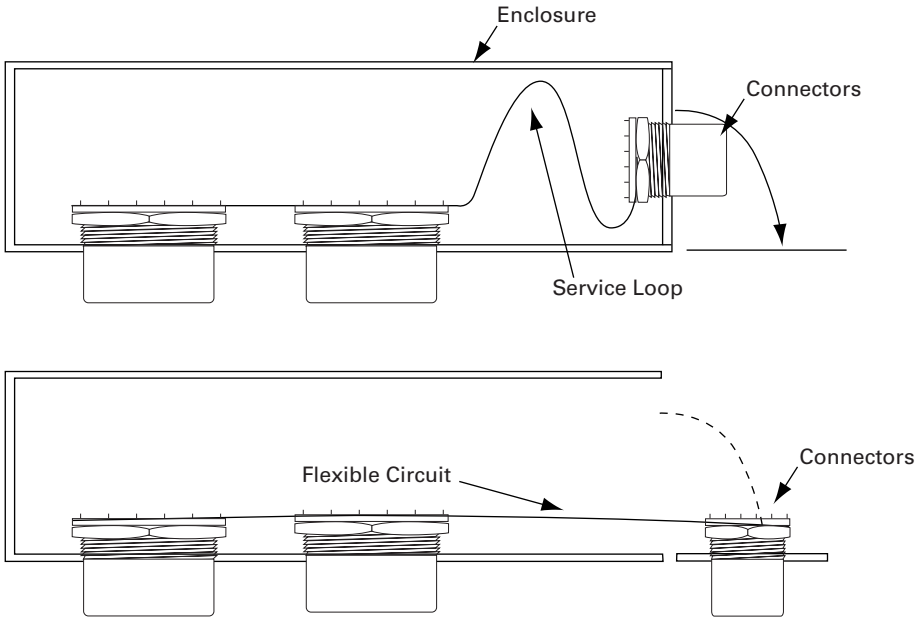


Figure 1-2. A service loop should be used when opening the package results in circuit flexing.

2

Flexible Circuits

Chapter Terms

Annular Ring: That portion of a conductive material completely surrounding a hole.

Barrel Cracks: Cracks that appear in the electro-plating inside a plated through hole due to mechanical and thermal stresses.

Basestock: The insulating material upon which a conductive pattern may be formed.

Base Material: See Basestock.

Blister: Delamination in the form a localized swelling and separation between any of the layers of a laminate base material, or between base material and conductive foil or protective coating.

Coefficient of Thermal Expansion (CTE): The linear dimensional change of a material per unit change in temperature.

Covercoat, Cover Lay or Cover Layer: The layer of insulating material that is applied over a conductive pattern on the outer surface of a printed circuit. Used for electrical insulation and environmental sealing.

Delamination: A separation between plies within a base material, between a base material and a conductive foil, or any other planar separation within a multi-layer printed board. See also Blister.

Dielectric: A material with a high resistance to the flow of electrical current.

DIP/Dual-in-Line Package: An IC package having pins that protrude through the substrate on which it is mounted. Electrical connection is usually made by soldering to the reverse side of the substrate to which the device is mounted.

Double-Sided Printed Board: A printed board with a conductive pattern on both of its sides.

Electro-deposited (Copper): The deposition of a conductive material (copper) from a plating solution by the application of electrical current.

Epoxy Prepreg: A glass impregnated epoxy adhesive material used to bond multiple layers, with high mechanical stability in all axes.

Etching: The chemical, or chemical and electrolytic, removal of unwanted portions of conductive or resistive material.

Flexible Printed Circuit: A patterned arrangement of printed circuitry and components that utilizes a flexible base material with, or without a flexible cover lay. See Flexible Printed Wiring.

Flexible Printed Wiring: A patterned arrangement of printed wiring and components that utilizes a flexible base material with, or without a flexible cover lay. See Flexible Printed Circuit.

Glass Transition Temperature (Tg): The temperature at which an amorphous polymer, or the amorphous regions in a partially-crystalline polymer, changes from being in a hard and relatively brittle condition, to being in a viscous or rubbery condition.

Hold-Down Tabs: Conductive tabs extending from the outside of an annular ring or other termination pad used to help secure the pad to the substrate.

Interfacial Area: The boundary between the flexible and rigid sections of a rigid-flex circuit assembly.

Modified Acrylic Adhesive: An adhesive material commonly used in multi-layer flexible circuits.

Multilayer Printed Board: The general term for a printed board that consists of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected.

Multilayer Printed Circuit Board Assembly: An assembly that uses a multi-layer printed circuit board for component mounting and interconnecting purposes.

Plated-Through Holes: A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board.

Polyimide: A dielectric film material commonly used for flexible circuit fabrication as an insulating layer.

Resin Recession: The presence of voids between the parallel of a plated-through hole and the wall of the hole as seen in microsections of plated-through holes that have been exposed to high temperatures.

Rigid-Flex Printed Board: A printed board with both rigid and flexible base materials.

Single-Sided Printed Board: A printed board with a conductive pattern on one of its sides.

SMD/Surface Mount Device: Any active or passive component packaged such that electrical and mechanical contact is achieved on the top surface only of the substrate on which it is mounted.

Terminal Pad: A portion of a conductive pattern that is usually used for making electrical connections, for component attachment, or both.

Through-Hole Technology: Techniques used to connect electrical components to a conductive pattern by the use of component holes.

Vertical Pins: A type of termination which connects two conductor runs in a solder assembly where the runs are in two different layers.

Vias: A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material.

What Is a Flexible Circuit?

In its simplest form, a flexible circuit is a pattern of conductors printed on a flexible dielectric (insulating) film. The technology to print electronic circuits on flexible materials was developed in the 1950's in response to the Space Program's need to save weight and space. The relatively simple single-sided and double-sided circuits from that time have evolved into multi-layer circuits and combination rigid-flexible circuit assemblies which provide total electronic packaging solutions. Applications for flexible circuits today span the full scope of the electronics marketplace — from military and aerospace, to telecommunications and computers; from industrial controls and process equipment, to automotive instrumentation; from consumer goods to toys. The expanding application for this technology fuels its evolution as a cornerstone in the quest for better electronic packaging.

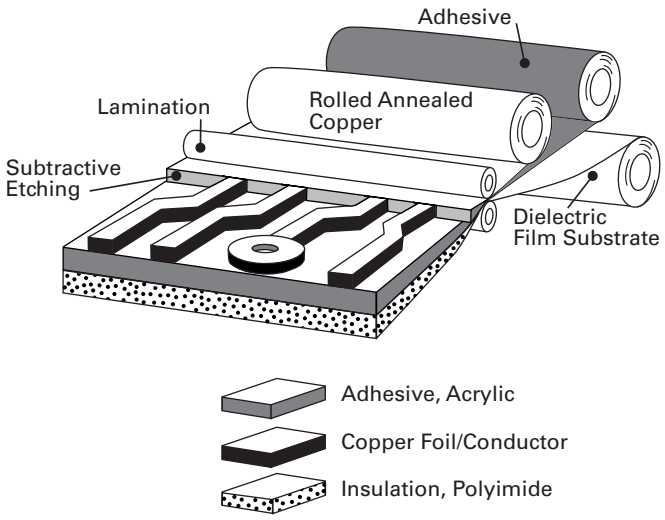


Figure 2-1. Basic flexible circuit construction.

Flexible circuitry can be designed to achieve maximum savings in assembly time, weight, space and cost. Flexible circuitry and rigid-flex circuits have a higher degree of reliability because of the decreased need for interconnection hardware normally used in conventional electronic packaging. Flexible circuit packaging reduces the chance of human error in installation and permits highly repeatable production assembly.

The Benefits of Flexible Circuits and How To Evaluate Them

In addition to the savings in assembly time, weight, space and cost, the flex conductor's flat form provides about 50% more surface area than a round wire of equivalent cross-section. This provides greater heat dissipation and a higher current carrying capacity. Smaller conductor widths using lighter weight materials and very thin insulating materials can be used to carry the same current to further aid in weight and volume reductions. The overall reduction in weight and volume expected can be up to 70% as compared to a similar design using conventional round wiring harness methods.

Despite the advantages, not every packaging problem can be economically solved by the use of flexible circuitry. There are several factors that must be examined to be sure that this type of packaging would be the most cost-effective and still meet all mechanical, electrical, and thermal parameters. If cost is a major concern, then the total installed cost of the competing interconnect system must be considered against using flexible circuitry in the electronic interconnect system. A correctly designed flexible or multi-layer flexible circuit can reduce not only weight and volume, but also the amount of connectors and other independent connection devices. The combined costs of the procurement, storage and assembly of all these independent pieces must factor into any cost evaluation.

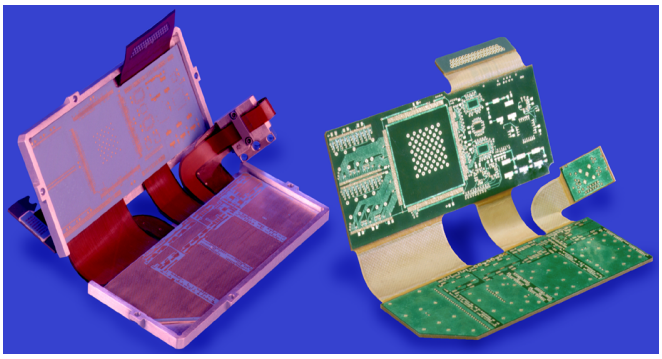


Figure 2-2. Comparison of "before" and "after" designs.

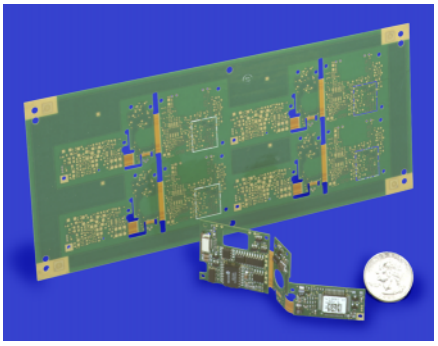


Figure 2-3. Quality engineered appearance example.

Overall circuit complexity and the total number of circuits that will be required must also be considered. If a circuit design is relatively simple, if total volume is low, and if space is available, conventional interconnect methods would likely be the most cost-effective. However, if the circuit is more complex, consisting of many signals or requiring specific electrical or mechanical requirements, then flexible circuitry would be the better design choice.

Major Types of Flexible Circuits

Flexible circuits can be designed and manufactured to meet a wide variety of interconnect requirements. From the simplest single-sided circuit, to multi-layer circuits with 40 layers or more, each is constructed using the same materials and techniques. Their materials and construction are described below.

Single-Sided Flexible Circuits

Single-sided flexible material with or without shield(s) or stiffener(s) (one conductor layer)

The single layer flexible circuit is the simplest and easiest to manufacture and is used primarily for point-to-point wiring. A wide choice of conductor thickness, widths and shapes, as well as connector attachments and termination pads are available. It is usually constructed of a single layer of copper foil laminated to a flexible substrate insulating dielectric film. Another layer of flexible dielectric film, known as the covercoat, is laminated to the imaged and etched copper substrate, encapsulating the conductors to provide electrical insulation and protection from the environment. The design of a layer of circuitry for a single layer can be as simple as a solid copper plane with only one solderable connection, to a multitude of conductors and terminal pads spread over a sheet as large as 24 X 30 inches (610 X 762 mm). Multiple single layers can be used together to make a complex assembly that consists of interconnects using either pins, connectors or other electrical components. Single-sided circuits can be supplied in different ways to meet specific application needs. Refer to Figure 2-4.

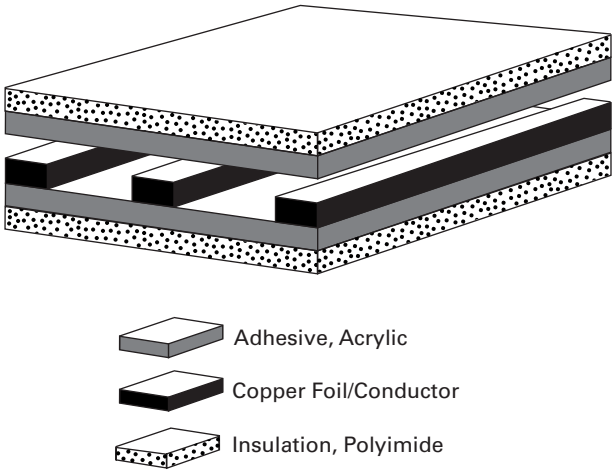


Figure 2-4. Single-sided circuit construction.

There are three basic types of single-sided flexible circuits, presented in order of increasing cost – single access uncovered, single access covered, and double access covered. Each is described as follows.

THE BASICS

BASIC FLEX CIRCUIT MATERIALS

There are a number of materials used in the manufacture of flexible circuits. Please refer to the *Materials* Section for detailed information regarding these materials. This is basic information on the material types used to aid in an understanding of this section on the types and construction of flexible circuits.

There are three fundamental types of materials used in fabricating flexible circuits — conductor, dielectric or insulator film, and adhesive. Each is described below.

Conductors — Copper foil is the conductor material of choice with the electrical and physical properties necessary to withstand both the manufacturing processes and the environments in which flexible circuits are typically used. The copper foil is bonded to a base dielectric or insulator film material using an adhesive film. The copper foil is typically coated with a photo-sensitive layer which results in the desired pattern of conductors and termination pads after exposure and etching processes.

Dielectric or Insulator Film — Dielectric or insulating films are used to provide the base on which the copper foil conductor layer(s) are attached. The most common dielectric film material is polyimide.

Adhesives — Adhesive films provide the material to bond the copper foil to the base film. An adhesive film layer is sandwiched between the copper foil and dielectric base film, and the multi-layer "sandwich" is laminated using heat and pressure.

Access Methods

Access to a pattern is accomplished in one of two ways, depending on whether access to one or both sides of a pattern is required. Each method is described as follows.

To gain access to one side of a pattern, holes are pre-drilled in the base dielectric film or covercoat prior to laminating the copper foil. The artwork pattern must be accurately positioned to match the location of the pre-drilled holes from the copper side. Since the operator cannot see the pre-drilled holes through the copper, this alignment must be accomplished using alignment pins. The circuit is then covercoated using a pre-drilled covercoat in the same manner as a single access covered circuit. Refer to Figure 2-5.

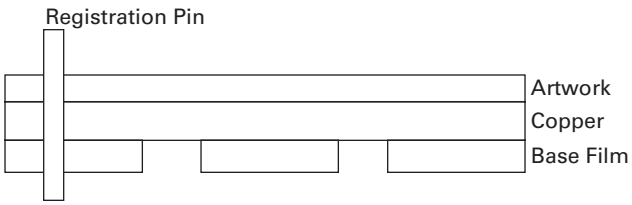


Figure 2-5.Access Methods

Single Access Uncovered

This type of single layer flexible circuit is the most inexpensive. It consists of a base dielectric film and copper foil that is imaged and etched. Because there is no protective covercoat laminated to the etched pattern, the expense of the covercoat and processing is eliminated. This type of circuitry is normally used in applications where the circuit will not be exposed to an adverse environment or to harsh mechanical abuse. Typical applications are telephones, toys and other consumer goods which are typically small, enclosed items. Refer to Figure 2-6.

Single Access Covered

Circuits made using this method are the same as the single access uncovered, except for a flexible dielectric film laminated to encapsulate the conductors for both electrical insulation and protection from the environment. The pre-drilled holes are aligned to the terminal pads prior to covercoat lamination to provide access to the pads. Refer to Figure 2-7.

Double Access Covered

This type of single layer circuit, known also as reverse bared, is the most expensive of the three single-sided assembly techniques. It allows access to a circuit from both sides, while also providing the environmental protection of insulating material on both sides of the copper conductors. Refer to Figure 2-8.

Access to both sides of a single layer flexible circuit is achieved by milling the covercoat material from the base material with a laser after the covercoat is applied. This process will yield near-perfect registration to the pad, but is tedious and time consuming. Both of these methods increase the circuit cost because of increased labor and decreased yields. Refer to Figure 2-5.

There are several folding techniques that can be employed to reduce or eliminate the need for reverse baring of the solder pads. Each reduces or eliminates the need for reverse baring of the solder pads by physically moving the bottom access to the top plane. These methods are shown in Figure 2-9 and should be considered prior to designing a circuit requiring reverse baring.

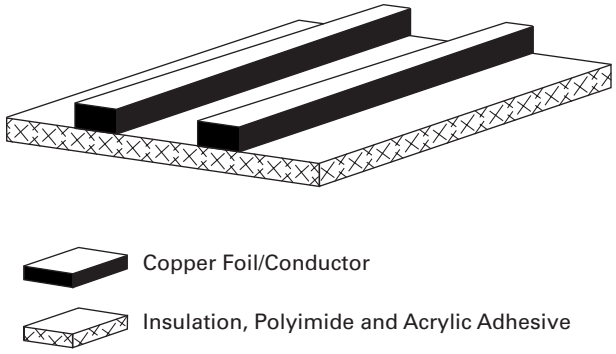


Figure 2-6. Single access uncovered circuit construction.

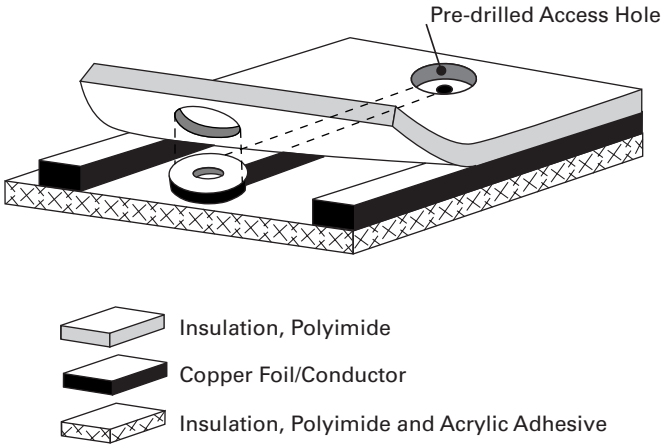


Figure 2-7. Single access covered circuit construction.

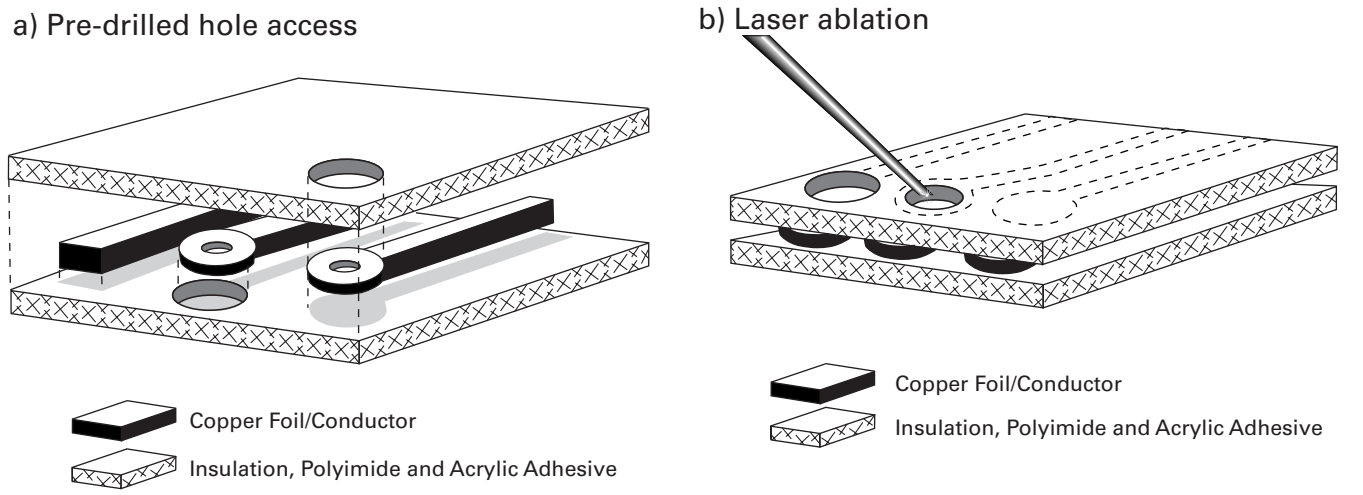


Figure 2-8. Double access covered circuit construction; a) pre-drilled hole access; b) laser ablation.

Double-Sided Flexible Circuits

Double-sided flexible material, with or without shield(s) or stiffener(s) (two conductor layers); with plated-through holes

A double-sided flexible circuit allows for more complex point-to-point wiring using almost the same space as a single-sided flex circuit. Double-sided circuits consist of a flexible base dielectric material with copper foil laminated to both surfaces. This allows for a design that utilizes conductors on both sides of the dielectric substrate for more efficient packaging. The conductors can be connected electrically by using plated-through hole technology. A flexible insulating dielectric is used to encapsulate the etched pattern to provide electrical insulation and protection from the environment. This covercoat material must have the terminal location hole drilled prior to lamination to allow access to the terminal pads. Refer to Figure 2-10.

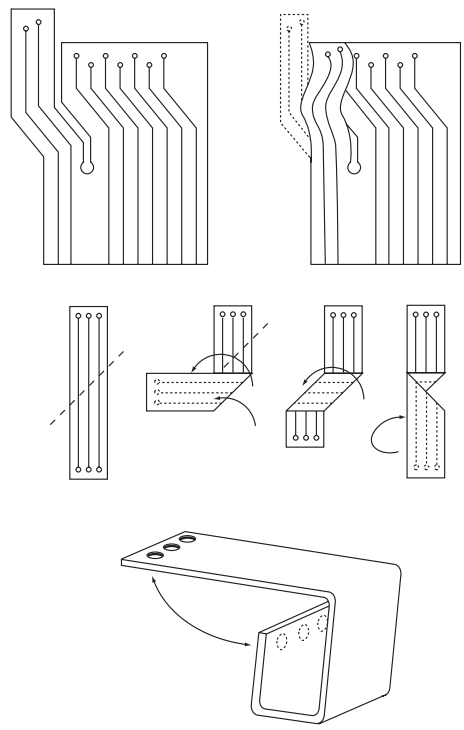


Figure 2-9. Techniques used to reduce need for reverse baring of solder pads.

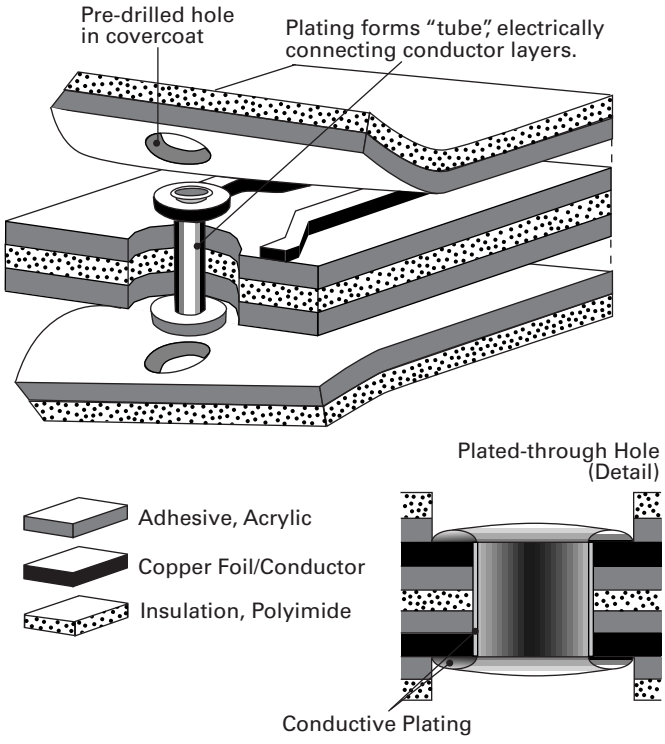


Figure 2-10. Double-sided flexible circuit construction.

When the circuit is designed to use plated-through holes, hold-down tabs on the terminal pads are not necessary, since the plating provides support to the pad area. This means that a higher density design can be achieved in the termination area without violating any conductor-to-pad spacing requirement. Unsupported or non-plated pads require hold-down tabs to provide the necessary mechanical support.

Multi-layer Flexible Circuitry

Multi-layer flexible material, with or without shield(s) or stiffener(s) (more than two conductor layers); with plated-through holes

Multi-layer circuits allow very high density packaging using complex point-to-point wiring. They can integrate systems requiring multiple interconnections into one unit, thereby reducing assembly time, cutting weight and volume, and increasing reliability. Typical applications for these types of circuits are those that must have shielded conductors, where impedance control is necessary, or where several layers of circuitry must access different areas. Because all holes can be drilled and plated-through, a designer can access several internal pads or circuit layers on each connector pin without having to use multiple soldering operations. Refer to Figure 2-11.

Multi-layer flexible circuits can be designed to meet most of the electrical, mechanical and environmental conditions found in both military and commercial applications. These technologies provide a wide choice of conductor configurations and terminations. They can be designed with as few as four layers, or to 24 or more layers. Each of these types is discussed separately to show their particular benefits and constraints.

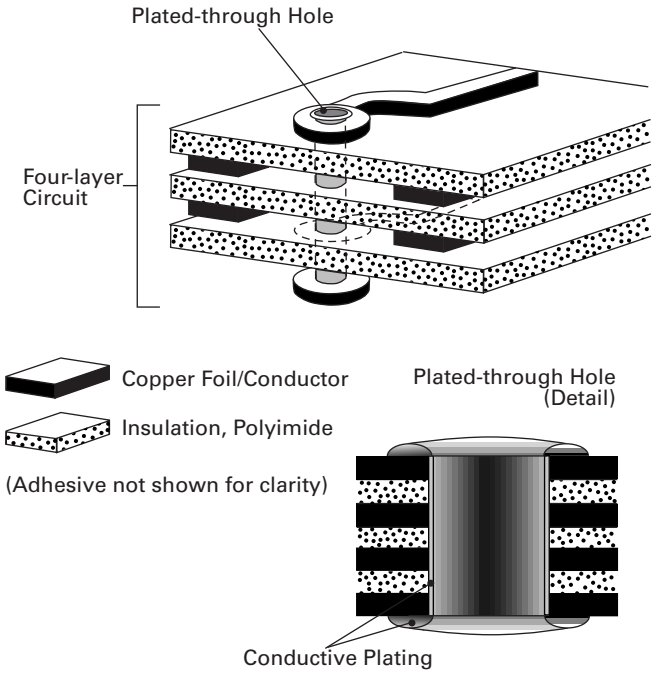


Figure 2-11. Multi-layer circuit construction.

Multi-layer flexible circuits consist of multiple single- or double-sided flexible circuits laminated together to form an integral component. They can be bonded over their entire surface or bonded only in selective regions to allow increased flexibility, as shown in Figure 2-11. When fully bonded, multi-layer circuits become increasingly less flexible as the number of conductive layers increases. Full bonding is recommended only with four or fewer layers. When more layers are required, the bonding adhesive should be removed in sections designed to bend or form.

A variety of insulating materials is available for inner-layer substrate and covercoating of the flexible layer. The most commonly used is polyimide film, which is available in thicknesses ranging from 0.001" to 0.005" (25µm to 125µm), with modified acrylic adhesive thicknesses ranging from 0.001" to 0.003" (25µm to 75 µm). Other thicknesses are available at extra cost, but should be considered only for special requirements.

The most common copper weights used in multi-layer flex circuits are 1 oz. (35µm) and 2 oz. (70µm); Teledyne has produced circuits using 6 oz. (210µm) copper. Since flexibility decreases as the copper weight increases, designs should specify the thinnest copper possible without compromising electrical requirements.

The various methods of processing multi-layer flexible circuits each have their advantages and disadvantages. In fully bonded circuits for example, double adhesive-coated insulating material, usually polyimide film, can be used to bond layers together, which eliminates the need for covercoating individual layers, cutting both material and labor cost. But, as previously noted, the number of layers that can be laminated together and still maintain flexibility is limited. To achieve flexibility with higher layer counts, selected areas are left unbonded. Those areas which are bonded, however, must do so where the layers are already covercoated using a modified acrylic adhesive. This is a significant source of mechanical failure because the bond strength between a processed polyimide film covercoat and acrylic adhesive is marginal and subject to delamination. In addition, the acrylic adhesive is thermally unstable in regards to low Tg, and high CTE. When used in a board requiring plated-through hole processing, this introduces a variety of problems ranging from barrel cracks to resin recession. These problems compound as circuit thickness

increases due to the added acrylic adhesive. To ensure thermal stability, materials are used which possess very high glass transition temperatures (Tg) and low coefficient of thermal expansion (CTE). Please refer to the discussion of *REGAL® Flex* later in this section for the best procedure for designing a thermally stable multi-layer flexible circuit.

Rigid-Flex Circuitry

Multi-layer, rigid and flexible material combinations (more than two conductor layers); with plated-through holes

Rigid-Flex circuits, like multi-layer circuits, allow very high density packaging using complex point-to-point wiring, can integrate systems requiring multiple interconnections into one unit, and can provide significant reductions in assembly time, weight, and volume, while increasing reliability. Typical applications for rigid-flex circuits are the same as for multi-layer circuits. Unlike multi-layer circuitry, rigid-flex circuits can have both surface-mount and through-hole components mounted in rigidized areas without risking damage from flexing. Again, like multi-layer circuits, rigid-flex circuits can be designed to meet most of the electrical, mechanical and environmental conditions found in both military and commercial applications, providing a wide choice of conductor configurations and terminations, with as few as four layers, or to 24 or more layers. Refer to Figure 2-12.

A rigid-flex circuit consists of multiple flexible wiring layers, selectively bonded together using an adhesive. A cap layer of rigid core, copper clad laminate is bonded to the top and bottom of the circuit to further add stability to the bonded areas. It is in these bonded areas that the circuit board will be drilled and plated-through to provide the necessary Z-axis interconnects between the flexible wiring layers. Components are mounted on rigid sections. Figure 2-12 shows the traditional construction used for most applications.

As shown in Figure 2-13, the flexible printed wiring (inner) layers consist of a flexible base dielectric with rolled annealed copper bonded on one or both sides. Because of its grain structure, rolled annealed copper is more flexible than electro-deposited copper. After this substrate is imaged and etched using conventional processing equipment, a cover layer dielectric is applied to encapsulate the copper traces. This covercoat electrically insulates the conductors and shields them from the environment.

Rigid-flex assemblies can only be manufactured using this process and these materials in limited quantities. The flexible dielectric materials used in their manufacture have properties that make these materials unsuitable for multi-layer processing. First, the acrylic adhesive

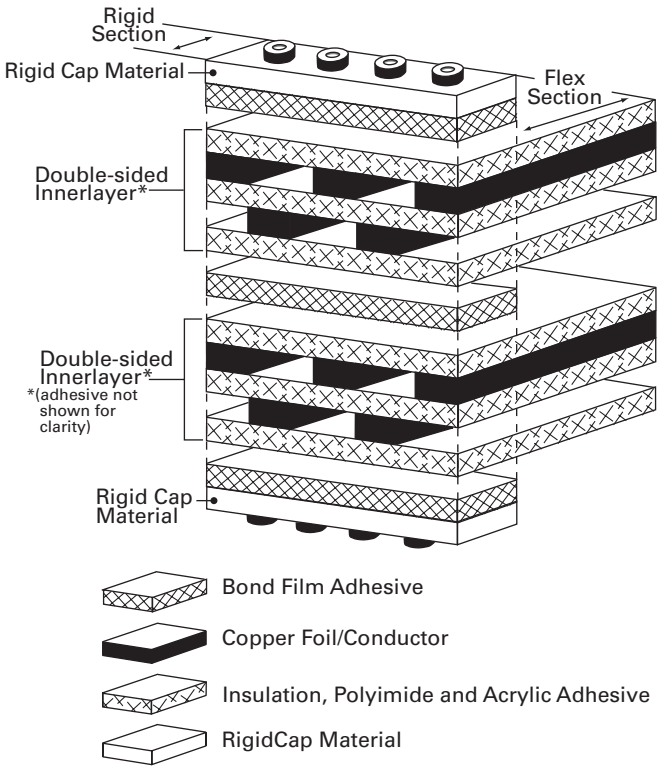


Figure 2-12. Traditional rigid-flex circuit construction.

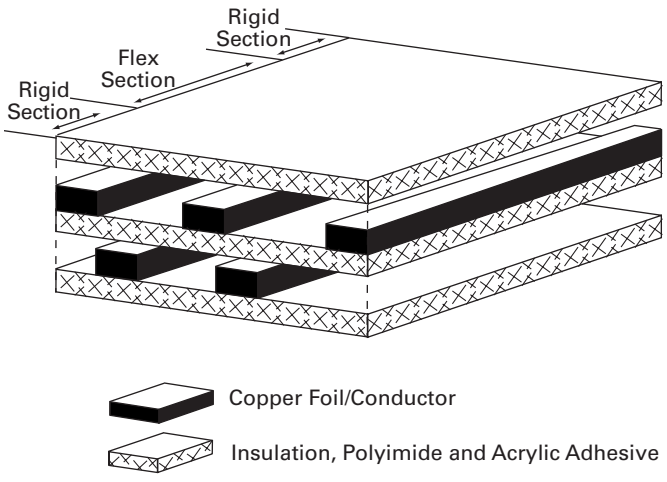


Figure 2-13. Traditional rigid-flex innerlayer construction.

Material Characteristics

Material	Moisture Absorption (% by Weight)	CTE Z Axis (ppm/°C)	Tg (°C)
Acrylic Adhesive	4	425	40
Epoxy Prepreg	2.2	85	130
Polyimide Film	1.33	48	390
Polyimide Prepreg	0.7	55	210
High Tg Epoxy Prepreg	1.75	70	170

Table 2-1. Shows comparative data for several materials for both moisture absorption and CTE.

has a high moisture absorption characteristic of approximately 4% by weight. The polyimide film also absorbs moisture, but at a lower rate of approximately 3% by weight. Moisture absorption affects the multiple layers in two ways. The basestock itself is unstable in the X and Y axis because of the growth and shrinkage of the material due to the moisture content, leading to a layer-to-layer registration problem during lamination on high density circuit boards. Moisture also affects the quality of the circuit board by outgassing during extreme thermal rises, such as soldering. Outgassing of moisture causes delamination, resin recession and "blow outs" in the plated-through holes. Moisture can be driven out of the material by proper pre-baking of the circuit prior to any temperature excursions.

Another property of the acrylic adhesive that makes it unsuitable for use in multi-layer boards is its high coefficient of thermal expansion (CTE) above its glass transition temperature (Tg) — the CTE of acrylic is approximately 425 ppm/°C as compared to 70 to 85 ppm/°C for most epoxy prepreg materials. This high CTE means that the material has a high Z-axis expansion rate. During thermal rises the acrylic adhesive expands at a higher rate than the other materials used in the construction. Defects such as barrel cracks, outer layer pad lift, and delamination can result from the thermal instability of the acrylic adhesive.

To achieve increased reliability and higher layer counts, the amount of acrylic adhesive must be limited or eliminated in the rigidized areas. This can be accomplished by processing the innerlayer basestock on a polyimide/acrylic base and then using a selective covercoating method whereby the polyimide/acrylic adhesive material is laminated in the flex area only. The conductor traces in the board area are covercoated using an epoxy prepreg. Refer to Figure 2-14.

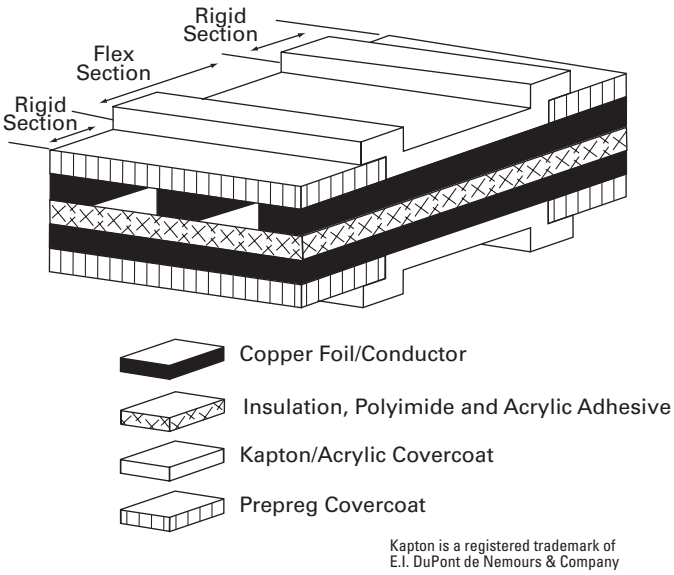
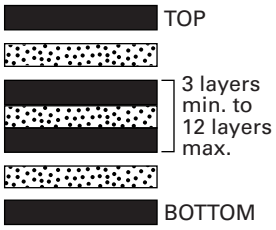
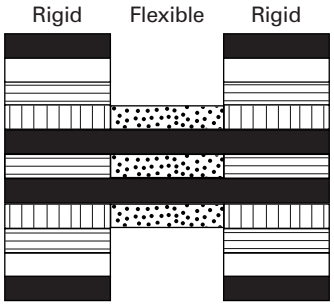
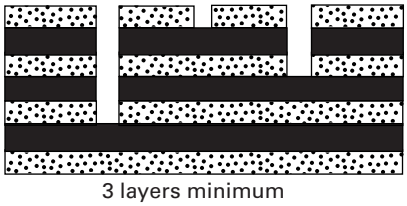


Figure 2-14. Hybrid rigid-flex inner layer.

To provide electrical insulation reliability, the manufacturer must engineer into the tooling scheme an overlap of these separate dielectrics to prevent shorting between subsequent layers and to ensure environmental sealing. By using prepreg bond films to bond all the layers together, the amount of acrylic adhesive is further reduced. This technique allows the use of polyimide/acrylic materials to be minimized in the rigid areas of the circuit board. The major drawback to this construction is the X- and Y-axis instability of the base material, which leads to problems with layer-to-layer registration during final lamination.

Types of Flexible Circuits

Type	Common Name	Layer Composition
1	Single-sided	
2	Double-sided, plated through holes	
3	Multi-layer, flexible plated through holes	
4	Rigid-flex, multi-layer with plated through holes	
5	Multi-layer, no plated though hole	

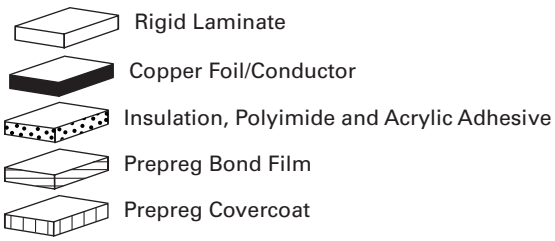


Table 2-2.

REGAL® Flex

Teledyne Electronic Technologies has successfully developed a process that completely eliminates all polyimide films and acrylic adhesives in the hardboard areas of a rigid-flex circuit. This patented manufacturing process, known as REGAL® Flex, produces a rigid-flex assembly that is thermally stable and offers ultra-high density.

REGAL® Flex 1

The REGAL® Flex process substitutes the polyimide/acrylic base materials normally bonded to the selected copper, with an epoxy prepreg material to create a single or double-sided clad base laminate. Coverlays of polyimide/acrylic materials are then registered and laminated at flexible areas only, after image and etch operations are complete. These circuit layers can now be stacked for multi-layer circuit lamination using epoxy prepreg bond plies, registered in place at the rigidized sections of the circuit. Refer to Figure 2-15.

This process results in a more stable x, y and z-axis circuit for component assembly at the rigidized sections by eliminating the higher moisture content materials from these areas. The flex area is slightly less flexible due to the prepreg usage on the base stock. However, final flexibility exceeds flex-to-install requirements and provides for a lower cost lamination process.

The resulting covercoated layers are then selectively bonded using a pre-windowed epoxy prepreg bond film to allow for rigidizing selective areas for subsequent through-hole processing. The methods used to produce this type of rigid-flex board are the same as those used to manufacture an all polyimide film/acrylic construction board. The major difference is the materials used when processing.

Both of these manufacturing techniques can be used on applications that require the flexible section to bend during installation, normally not more than 90°. Circuit boards manufactured using these techniques have exceeded the military specification for a flex-to-install application of 25 or more flexing cycles.

REGAL® Flex 5

When flexibility requirements of the application require a bend radius equal to or greater than industry standards (refer to the *Mechanical Design* Section) for higher layer count rigid flex applications, REGAL® 5 processed laminates are recognized industry-wide as the ideal construction method. REGAL® 5 laminates pro-

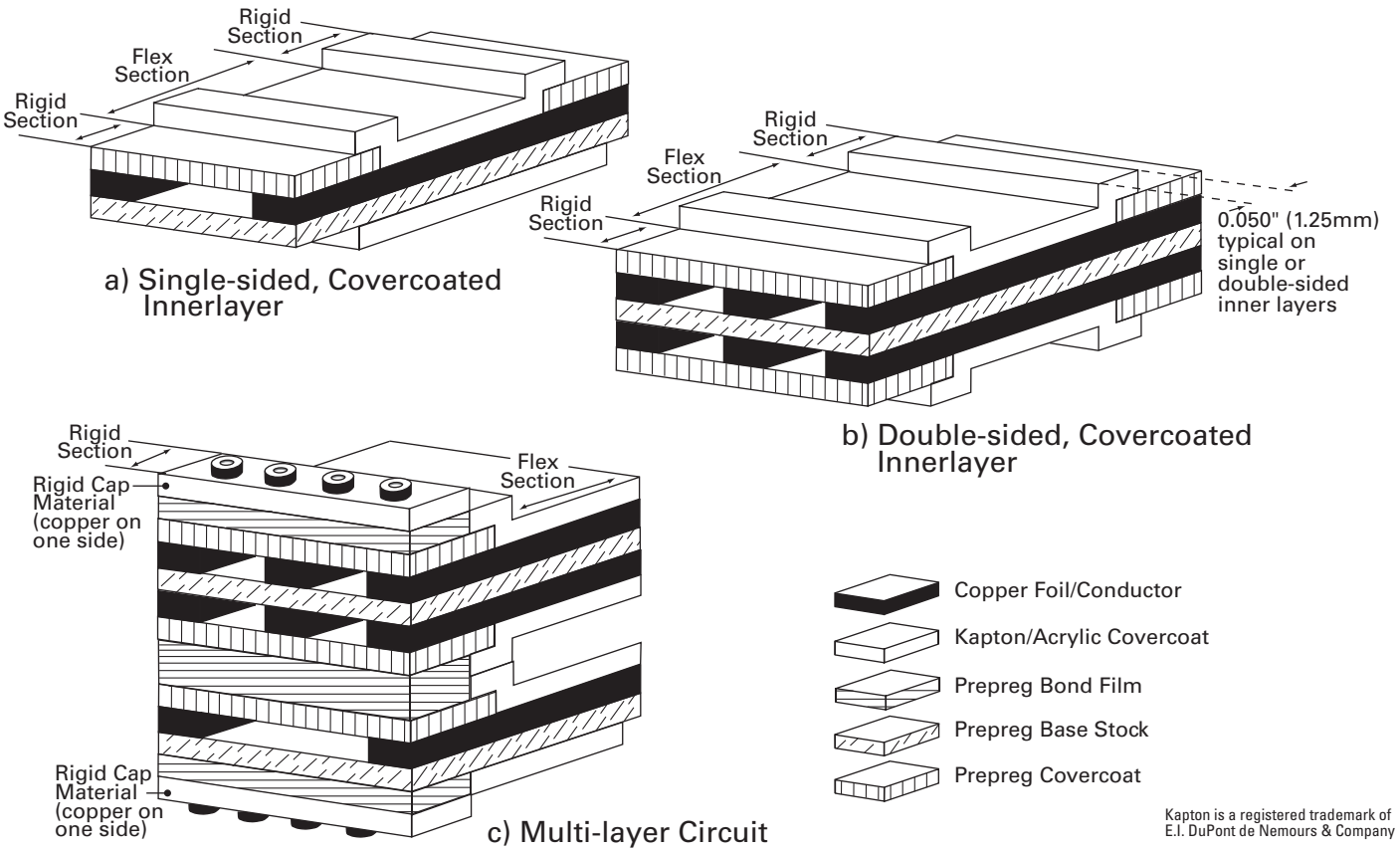


Figure 2-15. REGAL® Flex 1 construction; a) single-sided covercoated innerlayer; b) double-sided covercoated innerlayer; c) multi-layer circuit.

vide a more homogeneous laminate in both the rigid and flexible areas. Teledyne accomplishes this be manufacturing dual core material innerlayers, which result in no polyimide or acrylic materials in the rigidized areas of the board, while assuring this material remains in the flexible areas to provide maximum flexibility. Refer to Figure 2-16.

These dual core material layers are selectively bonded together using the same manufacturing processes used to build the other rigid-flex constructions previously outlined. By utilizing this manufacturing technique, an ultra-high density, highly reliable, and thermally stable rigid-flex circuit can be designed and built in large quantities.

As with the REGAL® 1 construction technique, REGAL® 5 rigid-flex can be manufactured with single-sided or double-sided innerlayers. Single-sided innerlayers offer increased flexibility for certain applications, and the ability of having an odd number of flexible inner layers. REGAL® 5 double-sided innerlayers provide the option of having the increased flexibility of all thin-film flex materials in the flexible section, along with the option of two conductive layers bonded to a shared dielectric. This technique will enhance the performance of designs incorporating controlled impedance or other transmission line electrical properties that require multiple innerlayers with shielding.

There are some distinct advantages to the REGAL® Flex processing method when compared to other rigid-flex construction techniques:

- In particular the thermal stability of REGAL® Flex circuit boards; acrylic adhesives have a glass transition temperature (Tg) of 40°C and a CTE of 400-600 ppm/°C. The Z-axis expansion of a rigid-flex using acrylic adhesive materials above Tg increases as the number of layers increases. The materials in a REGAL® Flex board have very specific thermal properties — the epoxy prepregs used have a Tg of 170°C and a coefficient of thermal expansion (CTE) of 70 ppm per degree C in the Z axis. The use of these materials yields a circuit board capable of passing a 290°C solder float for 10 seconds without exhibiting delamination or barrel cracks in the plated-through holes. This is due to the reduction in the Z-axis expansion rate of the laminated board. These advantages come at a

cost increase between REGAL® 1 and REGAL® 5 due to the increased processing complexity.

Conventional rigid-flex materials use a non-reinforced polyimide film as the base material. Since this material is dimensionally unstable during the manufacturing process, larger pad diameters on internal layers are required to compensate for the growth or shrinkage of the materials during processing. The increased pad diameters are needed so that after final lamination the manufacturer will have a greater chance of drilling down into the innerlayer pad at the drilling stage. It can be expected that a rigid-flex circuit incorporating an acrylic adhesive construction will exhibit high losses at the assembly stage due to delamination and barrel cracks. Because of the thermal stability of the REGAL® Flex materials, the board has the potential ability to withstand multiple wave solder operations without concern for creating failures.

REGAL® Flex innerlayers are constructed of a reinforced epoxy and fiberglass material that is woven to enhance X- and Y-axis stability. Because of the improved X- and Y-axis stability of the materials used when processing the innerlayers, multi-layer rigid-flex circuits designed for REGAL® Flex can achieve denser packaging. Smaller internal pads can be used along with tighter hole-to-hole spacing, which permits increased density and lower layer count.

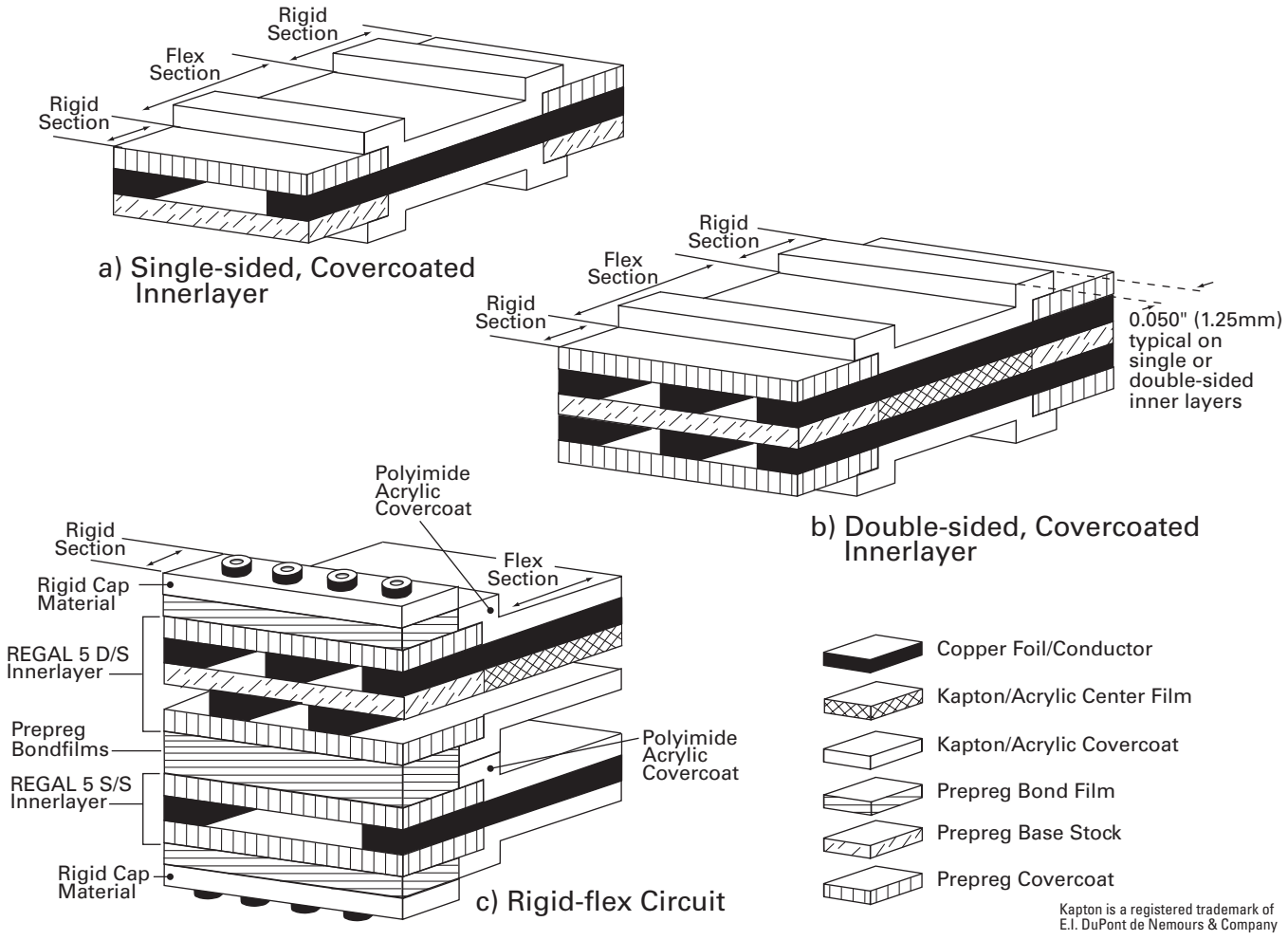


Figure 2-16. REGAL® 5 construction; a) single-sided covercoated innerlayer; b) double-sided covercoated innerlayer; c) rigid-flex circuit.

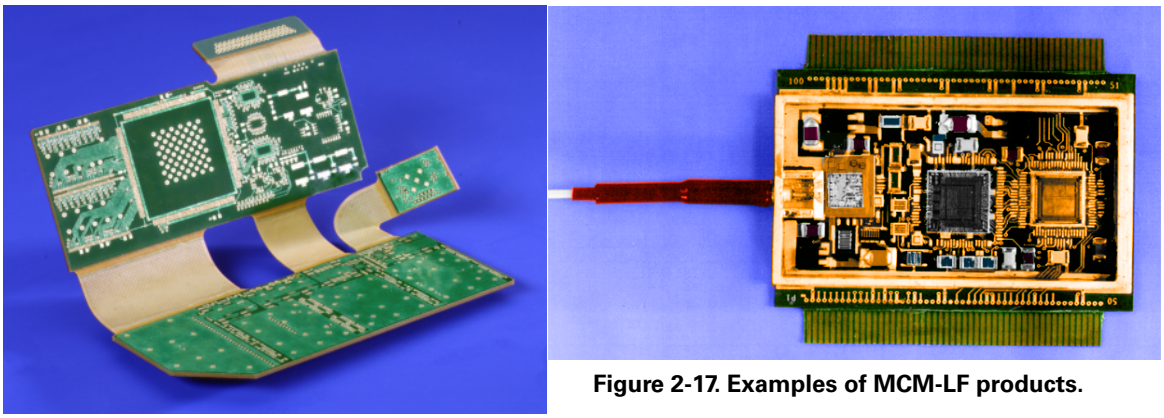


Figure 2-17. Examples of MCM-LF products.

Multi-Chip Modules (MCM)

Multi-Chip Modules (MCMs) can be defined as structures consisting of two or more integrated circuit chips that are electrically connected to a common circuit base and interconnected by conductors within that base. There are three basic types of technologies that are used to manufacture MCM structures. The differences between the competing technologies are the dielectric materials and the processes used to manufacture the structures. The three types are as follows:

MCM-C – modules constructed on ceramic substrates using thick film (screen printing) technologies to form the conductor patterns.

MCM-D – modules whose interconnects are formed by thin film deposition of metals onto deposited dielectrics.

MCM-L – modules using advanced forms of printed wiring board technologies to form copper conductors on laminate based dielectrics. Refer to Figure 2-18.

The benefits of Multi-Chip Modules are:

- Increased system speed
- Reduced overall size
- Ability to handle chips with large numbers of I/O's
- Reduced number of external connections

Of the three types of MCM, laminate-based Multi-Chip Modules (MCM-L) offer the end-user the lowest cost, especially for higher volume applications. Lower costs are achievable because of lower raw material and processing costs, and through the use of large format array processing. Other benefits of MCM-L technology include two-sided assembly for both Chip-on-Board and surface mount components, large area substrates, and the reduction of connectors through the use of rigid flex substrates.

One shortcoming of MCM-L technology has been achieving high interconnect density using conventional manufacturing techniques. High density MCM-L's may

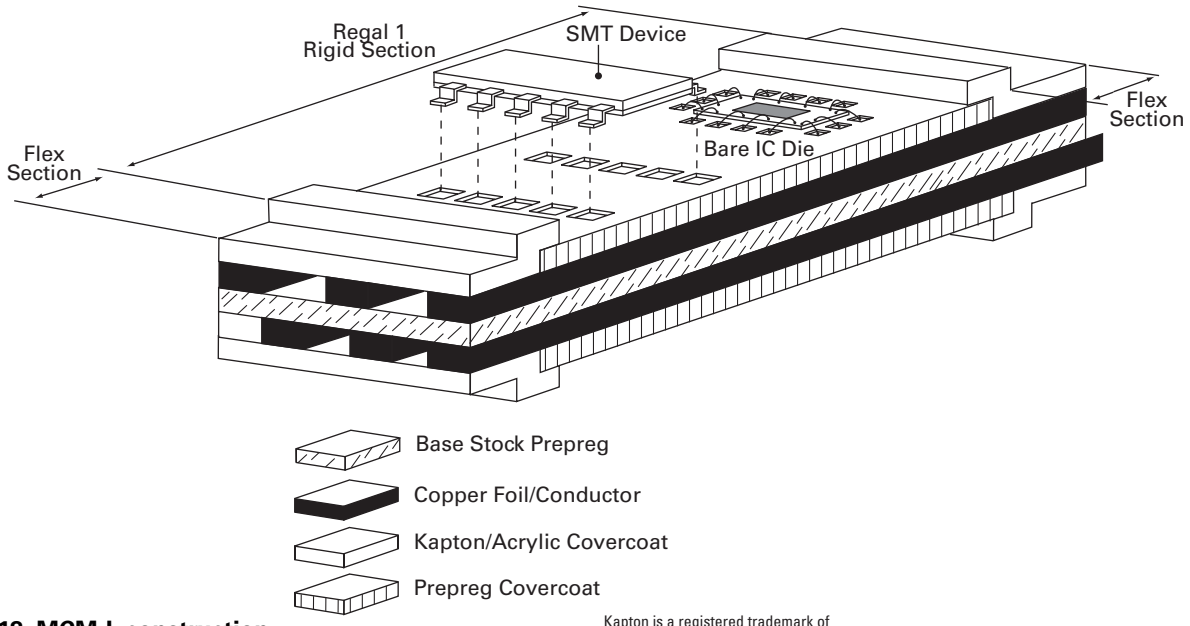


Figure 2-18. MCM-L construction.

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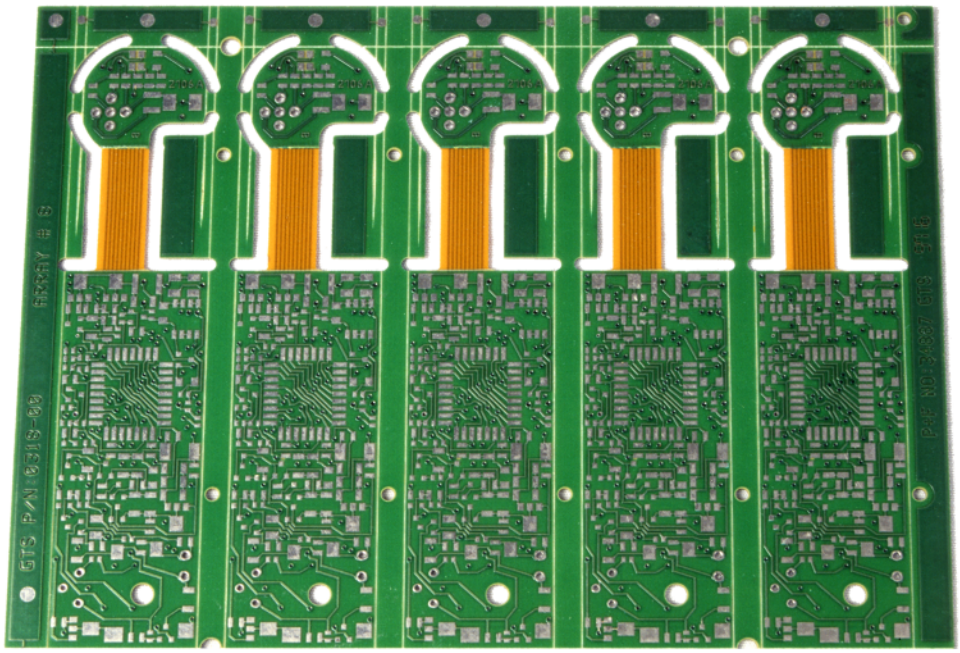
require additional design and engineering effort to obtain the interconnect density and performance required. To achieve the desired density, the design may incorporate smaller diameter drilled holes, blind and/or buried vias, and finer conductor widths and spacings. Many manufacturers are looking toward improved processing techniques and equipment to increase density. Processes such as micro-vias (vias less than 0.006" (150µm) in diameter) that are formed using advanced techniques such as laser drilling or plasma etching, and fine line imaging and etching will increase the circuit density without compromising yields.

Another area of concern is the relatively larger coefficient of thermal expansion (CTE) of the substrates. The thermal mis-match between the substrate and the die limits the size of the die that can be reliably bonded directly to a laminate substrate. The mis-match can be somewhat mitigated by the use of epoxy underfill beneath the die, or by using thermally matched substrates. Performance enhancements may also come from the use of thinner dielectric materials, low loss dielectrics and better thermal management techniques.



Product Example

3

Materials

Chapter Terms

Adhesiveless Laminates: A copper-clad laminate composite of polyimide film bonded to copper foil.

Basestock or Base Material: The insulating material upon which a conductive pattern may be formed. The basestock may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.

Covercoat, Cover Lay or Cover Layer: The layer of insulating material that is applied over a conductive pattern on the outer surface of a printed circuit. Used for electrical insulation and environmental sealing.

Electro-deposited (Copper): The deposition of a conductive material (copper) from a plating solution by the application of electrical current.

Flexible Soldermask: A soldermask that when cured over flexile circuits will not separate, fracture, or delaminate from that surface of the base material, conductors, and lands of the coated flexible wiring. IPC-TM-650, TM 2.4.29 specifies a minimum number of 25 cycles using a 0.125"(3.175mm) diameter mandrel.

LPISM: Liquid photo-imageable soldermask.

Reinforced Adhesive: An adhesive material whose mechanical strength is improved by the addition of glass fibers.

Soldermask: A resist that provides protection from the action of solder.

Tenting: The covering of holes in a printed board and the surrounding conductive pattern with a resist that is usually a dry film.

Thermoset Adhesive: An adhesive material that undergoes a chemical reaction when exposed to elevated temperatures that leads to it having a relatively infusable or crosslinked state that cannot be softened or reshaped by subsequent heating.

Conductive Materials

Thin copper foil is the most readily available and economical conductive material for flexible circuitry. Copper foil is available in two types, each with different properties.

The first type of copper foil is electro-deposited foil, which can be laminated to a dielectric to form base-stock. Some of the advantages of this type of copper foil are:

- economical
- rougher base bonding surface which enhances bonding
- vertical grain structure, which enhances fine line etching

The second type is rolled copper foil, normally available fully annealed, but also supplied as low temperature annealed. Rolled annealed copper foil is the type commonly used by flexible circuit manufacturers because of its flexing characteristics. Some of the advantages of this foil are:

- horizontal grain structure better suited for flexing applications
- can be supplied with a bond enhancer to aid in adhesion
- can be supplied with bond enhancer on both sides of the foil to reduce processing steps and handling
- can be double treated, which adds oxide treatment to the surface of the copper to greatly increase bond strength

Both foil types are readily available in various weights/thicknesses. Table 3-1 shows the more common thickness and their equivalent weights for a one square foot of copper foil of a given thickness. These foils are the easiest to handle and the most economical to process. They are readily available as straight foil, or can be pre-laminated to a base dielectric material.

COPPER FOIL THICKNESS AND WEIGHT COMPARISON

Weight	Thickness	
1/2 ounce	0.0007"	17µm
1 ounce	0.0014"	35µm
2 ounce	0.0028"	70µm
3 ounce	0.0042"	105µm

Table 3-1.

Surface Treatments

The surfaces of both copper types are normally treated by chemical oxidation to increase adhesion, to reduce resist undercutting by etchants, and to reduce bond degradation by plating chemicals. Electro-deposited copper is more easily treated and less expensive to treat than rolled copper. A thin layer of zinc applied to the copper foil's surface will increase bond strength and reduce corrosion. Other proprietary, stain-proofing treatments are also used.

Foil Grades

Copper foils come in a variety of quality and property grades. To avoid excessive foil defects, only the highest printed circuit quality electro-deposited copper should be used for flexible circuits. Both annealed and non-annealed electro-deposited copper foil are available. A special high ductility grade of electro-deposited copper called high tensile elongation (HTE) is available which possesses the physical property of increased elongation. Rolled copper is available in a special low temperature annealed (LTA) grade which is easier to handle and harder than ordinary soft rolled copper. LTA foil is annealed during lamination to a dielectric substrate.

The properties of electro-deposited and rolled, annealed copper are compared in Table 3-2.

PROPERTIES OF COPPER FOILS (1 OZ.)

PROPERTY	ELECTRO-DEPOSITED (High ductility)	ROLLED, ANNEALED
Purity	99.8%	99.9%
Resistivity (at 20° C)	16Ω g/cm²	15.2Ω g/cm²
Tensile strength @ 23°C	40kpsi	20kpsi
Tensile strength @180°C	20kpsi	14kpsi
Ductility elongation²	3%	10%
Standard weights	1/8 - 20 oz.	1/2 - 6 oz.

Table 3-2.

Other Metals Used in Printed Wiring Boards

Aluminum is used for electrical shielding or to replace copper in low cost circuits. It cannot be soldered or welded with conventional equipment.

Nickel, because of its hardness and ease of welding, is used to join components to substrates which cannot withstand ordinary solder temperatures. Both electroplated and rolled nickel are available.

Gold provides excellent corrosion resistance. Since it is extremely soft and very expensive, it is used sparingly, often as a plating.

Silver, with the highest conductivity of all metals, is frequently used as a contact material.

Copper Alloys: Phosphor bronze and beryllium copper foil provide circuitry with integral leaf springs and corrosion resistant contacts where precious metal plating is not required.

Ferrous Alloys: Soft ferromagnetic foils are used for magnetic shielding. Stainless steel foil is used for resistance heaters and circuits requiring high strength and corrosion resistance.

Nickel Alloys: Copper-nickel alloys, such as Monel®, are used for corrosion resistance. Nickel-chromium alloys, such as Inconel®, provide high electrical resistance for flexible heating elements.

Flexible Dielectric Materials

The design and use of flexible circuitry has been made possible by the availability of numerous flexible thin film dielectric materials. Each of these materials has properties which dictate where they are best used. When choosing a dielectric insulating film, there are many factors that should be considered, including operating environment, mechanical constraints of the material, electrical characteristics, and cost.

Some materials have qualities which make them well suited for the operating conditions of the final assembly, but they may not have the necessary chemical, mechanical or thermal properties necessary to withstand a manufacturing environment. To ensure that the correct material can be used for a particular application, overall environmental and manufacturing conditions to which the assembly will be subjected must be carefully analyzed.

Tables 3-4 and 3-5 list the characteristics of some high temperature thin film dielectrics. These films tolerate high

PROPERTIES OF VARIOUS CONDUCTIVE METALS

FOIL	ELECTRICAL RESISTANCE at 20° C		DENSITY	THERMAL CONDUCTIVITY	THERMAL EXPANSION COEFFICIENT	MATERIAL RESISTIVITY COMPARED TO COPPER*
	Ohms mil per ft.	micro ohms – sq. cm/cm	lb. per cubic inch	btu/hour/sq. ft./°F/ft.	ppm/ °F	
Aluminum	17	2.8	.097	118	13.0	1.635
Copper	10.4	1.7	.324	223	9.0	1.000
Gold	14.7	2.4	.698	170	7.8	1.41
Iron	60	10.1	.284	35	6.5	5.68
Lead	132	22.0	.410	20	16.3	12.69
Nickel	51	8.5	.322	35	7.0	5.77
Silver	9.8	1.6	.379	240	10.2	0.942
Tin	70	11.6	.264	35	14.9	6.73

*To compare resistance of material to that of copper of equal size.

Table 3-3.

CHARACTERISTICS OF THIN FILM DIELECTRICS

CHARACTERISTIC	UNIT OF MEASURE	POLYIMIDE FILM	FEP FILM	POLYESTER FILM
Dielectric Strength	V/Mil-1 Mil	4500	5000	7000
Dielectric Constant	1 kHz	3.4	2.1	3.1
Dissipation Factor	1 kHz	.0016	.0003	.005
Tensile Strength	PSI	20000	4000	25000
Elongation	%	70	300	100
Water Absorption	% By Weight	3	< .01	.8
Operating Temperature	°C	150	204	149
Absolute Max Temperature	°C	300	274	149
Low Temp. Embrittlement	°C	-55	-85	-50
Melt Point	°C	816	280	248
Weather Resistance	MIL-STD-2026	Excellent	Excellent	Fair
Fungus Resistance	MIL-E-5272	Non-Nutrient	Non-Nutrient	Non-Nutrient
Chemical Resistance	N/A	Excellent	Excellent	Excellent

Table 3-4.

volume assembly techniques, such as wave soldering, and multiple soldering operations without degradation.

Uses of Dielectric Films

When used on a flexible circuit, insulating dielectric films can function as a base film or a covercoat film.

The base dielectric film is used to support and protect the copper foil during the manufacturing process. It can also provide electrical protection (insulation) and environmental protection to the circuit. Different thicknesses of dielectric films may also be used to control impedance. The copper foil is bonded to the base dielectric prior to the imaging operation. The dielectric film therefore acts as an etch resist on the backside of the sheet on single layer flexible circuits. On double-layer applications, the base dielectric is sandwiched between two copper foils. This provides support and prevents etching on the backside of the copper foils.

The covercoat dielectric is thermally bonded to the base dielectric after the conductive pattern has been etched. The covercoat serves to protect the copper conductors from moisture, contamination and damage.

Adhesives

There are several types of adhesives from which to select, each with its own unique properties. The two main categories are thermoset flexible and reinforced adhesives. Within these categories are several choices. The selection of the proper adhesive and thickness to bond the conductive copper and dielectric is considered to be one of the most critical choices in flexible and rigid-flex circuitry design.

Thermoset Flexible Adhesives

Thermoset adhesives are used to bond flexible dielectric film to copper foil and to bond multiple layers together to form multi-layer flexible circuits. Two types of flexible thermoset adhesives — modified acrylic and epoxy — are available for processing flexible circuitry. They have different characteristics and are chosen for the specific application requirements.

Modified Acrylic Adhesive

Acrylic adhesives have been available for use in flexible circuitry manufacturing since the early 1970's. They

offer excellent adhesion to both the polyimide films and copper.

Typical bond strengths to treated rolled annealed copper are:

- 8-15 lbs./inch at room temperature
- 8-15 lbs./inch after solder float
- 7-14 lbs./inch after solder immersion

Other characteristics of acrylic adhesives are:

- thermal stability to resist multiple exposure to molten solder and hot oil reflow
- will pass UL tests for flammability at VO rating
- chemical resistance to withstand exposure to a wide variety of chemicals and solvents used in processing
- controlled flow of cover sheets and bond films
- easy processing
- batch-to-batch consistency
- excellent thermal resistance in heated environments
- repairability in the most demanding of environments

Modified acrylic adhesives do have some properties that adversely affect multi-layer circuit processing. First, their moisture absorption rate is approximately 4% by weight. Moisture can be successfully removed by baking prior to soldering. In multi-layer processing, however, adhesives are buried beneath several layers of other materials, requiring longer baking cycles to remove all the moisture.

Second, acrylic adhesives have a relatively low glass transition temperature (Tg), 40°C, and a coefficient of thermal expansion (CTE) of 400-600 ppm, higher than other bonding materials. When several layers of acrylic adhesive are used in a circuit board, such as in multi-layer flex and rigid-flex, these characteristics lead to defects. Z-axis movement of these materials can cause delamination and barrel cracks in plated-through holes.

Please refer to the *REGAL® Flex* discussion in Chapter 2 of this Design Guide to see how Teledyne has addressed these shortcomings.

Epoxy Adhesives

Prior to discovery of the superior flow characteristics, bond strength and temperature resistance of acrylic adhesives, modified epoxy materials were the material of choice for single-sided and double-sided flexible circuits. In multi-layer and rigid-flex circuits, however, epoxies are increasingly used because of their superior Z-axis expansion characteristics and lower moisture

FEATURE COMPARISON OF COMMON FILM MATERIALS

Property	Polyimide (Kapton)	FEP	Polyester
Tensile Strength	Very high	Low	Extremely high
Manufacturing Limitations	Few to none	Adhesion problems, low tensile strength	Sensitive to processing chemicals and soldering temperatures
Flammability	Non-flammable	Melts	High
Moisture Absorption	Highest	Lower	Lowest
Dimensional Stability	Unstable	Unstable	Stable
Flexible	Yes	Poorly	Yes
Bondable	Yes	Yes	Yes
Relative Cost	Moderate	Expensive	Inexpensive
Typical Use	Most widely used insulation	Excellent dielectric	Consumer-oriented

Kapton is a registered trademark of E.I. DuPont de Nemours & Company

Table 3-5.

absorption rate. Some of these epoxies also offer improved flexibility compared to acrylic based systems.

Bond strengths to treated rolled annealed copper are:

- 10-15 lbs./inch at room temperature
- 8-12 lbs./inch after solder float
- 8-12 lbs./inch after temperature cycling

Other characteristics of epoxy based adhesives are:

- thermal stability to resist multiple soldering operations
- chemical resistance to withstand multiple exposures to processing chemicals and cleaning solvents
- controlled flow
- batch-to-batch processing
- will pass UL tests for flammability at V1 or V0 rating
- moisture absorption rate as low as 1.5% by weight

Reinforced Adhesive Materials

Reinforced adhesives are made from glass bundles that are impregnated with either an epoxy resin or, in some cases, a polyimide resin. The materials are referred to as Pre-Impregnated Epoxy Glass, and Pre-Impregnated Polyimide Glass, respectively. These materials can be used in rigid-flex circuits as a bond film between layers, as a covercoat material, or as a base dielectric. Selected use of the materials allows for greater Z-axis expansion control. When used as a base dielectric, as in Teledyne's REGAL® Flex brand of rigid-flex, the flex layers have greater X- and Y-axis stability, resulting in better layer-to-layer registration.

Pre-Impregnated Epoxy Glass

Pre-impregnated epoxy glass, also known as "prepreg", can be used in rigid-flex applications as a bonding film, a covercoat or a base film, depending on the final application. Use of prepreg greatly reduces Z-axis expansion rates of a finished multi-layer circuit. Prepreg has a long record of proven reliability in the processing of rigid-style printed circuit boards.

Some of the characteristics of prepreg that warrant its use in rigid-flex are its higher Tg and lower CTE. The Tg of epoxy prepreg can range from 130°C to 170°C, with the Z-axis CTE at temperatures above Tg being approximately 115 ppm/°C. Substituting prepreg for acrylic adhesive (with a CTE of 400-600 ppm/°C), improves Z-axis stability significantly. Please refer to *REGAL® Flex* in Section 2 of this Design Guide for more information on the use of prepreg on rigid-flexible circuits.

Pre-Impregnated Polyimide Glass

Prepreg that is manufactured using a polyimide resin system can further enhance the thermal stability of plated-through holes in rigid-flex circuits. Polyimide prepregs have even better thermal characteristics than epoxy glass prepregs, with a Tg of about 200°C, and a Z-axis CTE of approximately 100 ppm/°C at temperatures above Tg. Their primary drawbacks are that they are more expensive, and have a shorter shelf life.

Adhesiveless Materials

Another construction technique available for the manufacture of rigid-flex circuits involves the use of adhesiveless polyimide materials. The adhesiveless materials are made by flowing a tightly controlled thickness of hot Kapton between two layers of copper, with the Kapton acting as the bonding agent between the two copper layers, thus eliminating the layers of adhesive materials described elsewhere. These materials simplify the construction of the final multi-layer circuit and reduce its overall thickness and weight. They possess a much lower coefficient of expansion than the adhesive materials. However, adhesiveless materials cost significantly more than other construction materials, and their shrinkage can be more difficult to predict. Also, impedance control can be more challenging because of the non-homogenous material stack up in the rigid areas.

Depending upon the application, though, an adhesiveless construction can be a viable option for producing rigid-flex circuits.

Soldermask

Soldermask can be used in the rigidized areas of rigid-flex circuits, using techniques and materials similar to those used on rigid boards.

The choice of soldermasks is determined by the application. Certain masks are preferred where wear resistance is important or where it is used as a dielectric. Others are better suited for SMT processes or as an environmental moisture barrier. The use of these coatings, and any special preparation or cleaning required prior to their application, should be reviewed for compatibility with other parts and materials used in the printed circuit board construction. These masks can be selected to meet commercial specifications (IPC-SM-840).

The conductive pattern to be coated can be prepared in one of two ways. The circuitry under the solder mask can either be solder (tin/lead) coated or left as bare copper. Of the two choices, soldermask over bare cop-

per (SMOBC) is preferred for two reasons. First, it results in a better bond; second, solder under soldermask could reflow during soldering causing electrical failures from solder bridging the conductors. SMOBC should be specified on the master drawing.

There are two types of soldermask that can be applied to the rigidized sections of a rigid-flex circuit. The soldermask can be supplied as a dry film, which is roll laminated onto the circuit, or alternatively as liquid photo imageable material (LPI), which is coated onto the circuit board. The dry film soldermask is supplied in rolls to the vendor and is hot roll-laminated onto the outer layers of the circuit. Imaging artwork is then used to expose the areas that are to remain by polarizing the film under bright light. The unwanted film is then rinsed away. With this dry film technique it is possible to attain tenting of vias. Some of the concerns regarding dry film soldermask include ionic contamination, flatness of the dry film, and, due to its relative thickness, problems with bonding over very dense conductor patterns and difficulties with fine pitch soldering. The film does not conform very well in dense patterns which could lead to cracking and peeling.

Liquid photo imageable (LPI) soldermasks are coated onto the surface by using either a curtain coating process, screening process, or spraying. LPI soldermasks bond very well to all features of the board because the liquid flows to cover all of the circuitry. The soldermask is applied and partially cured, then imaging artwork is used to polymerized and fully cure the mask in the desired areas. The unwanted mask is then stripped away. The major drawback of this soldermask technique is the inability to tent over via holes. After the soldermask has been applied and cured, all exposed copper surfaces can be solder hot-air leveled to facilitate subsequent component soldering.

Teledyne recommends that via holes either be completely open or completely tented with soldermask. Partially open vias can entrap processing fluids, either from fabrication or assembly operations, which can lead to reduced yields or premature field failures.

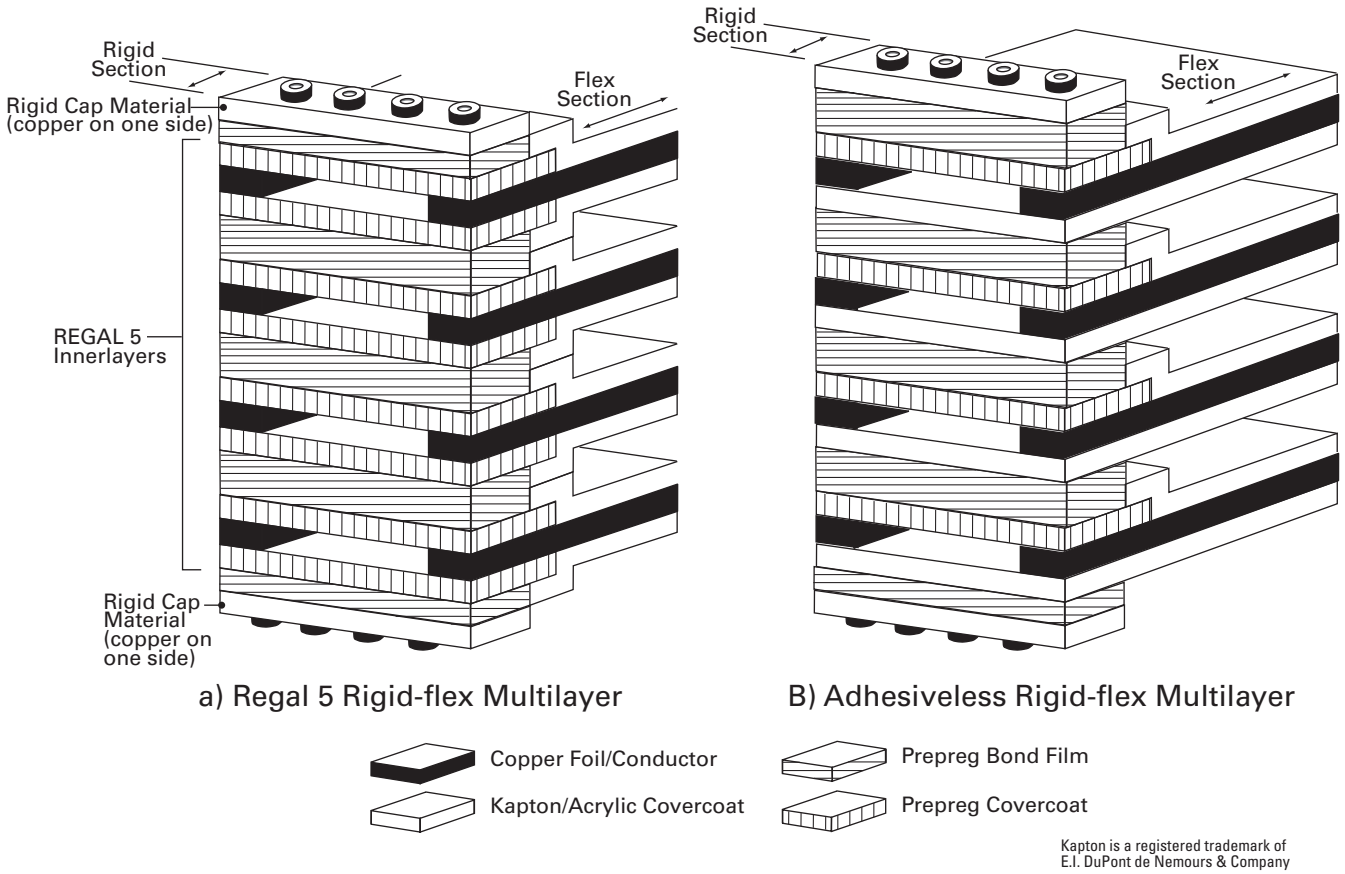
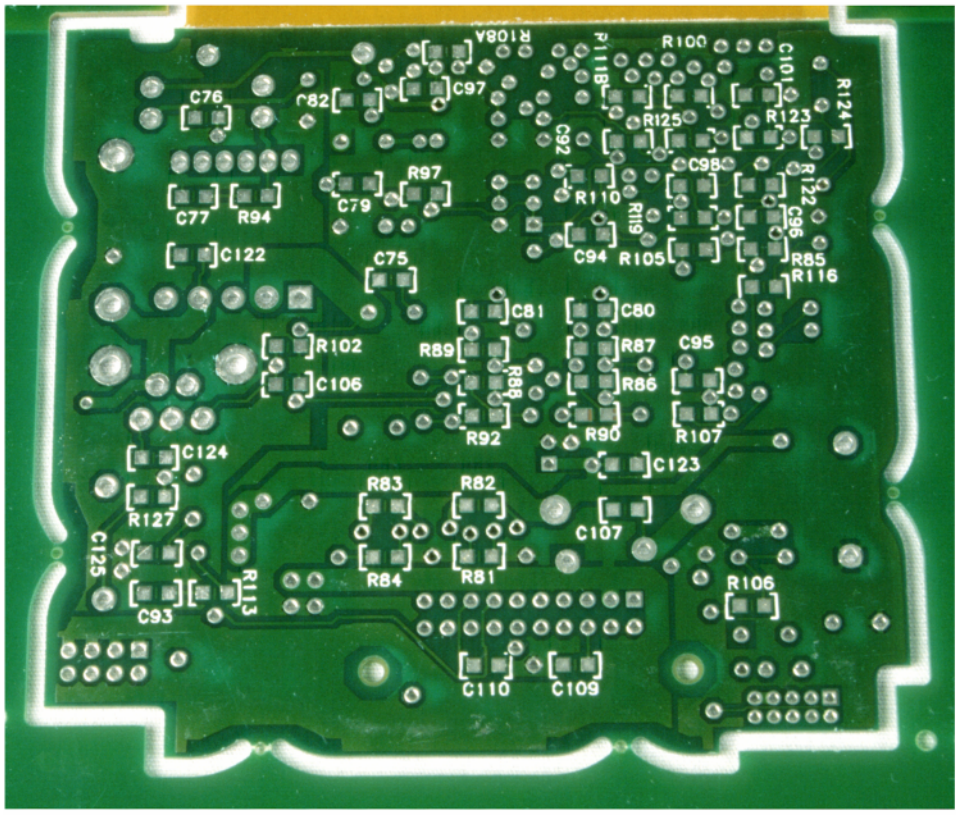


Figure 3-1. REGAL® 5 versus adhesiveless rigid-flex construction.

Flexible Soldermasks

Soldermasks are available that not only provide electrical and environmental protection but also are flexible enough to be used as a covercoat on a flex circuit. These soldermasks are applied using the same techniques described above, with the most prevalent being liquid photo imageable. The use of flexible soldermask may replace a traditional polyimide film covercoat for a lower cost with slightly lower performance.



Product Example

4

Electrical Design

Flexible circuitry is a custom-designed interconnection packaging device. Therefore, electrical requirements such as capacitance and impedance can be controlled. This section will discuss the decisions and trade-offs to be made during the design phase to meet all of the electrical, as well as mechanical, parameters of the circuit.

Conductor Thickness and Width

Copper foil is the material of choice for the majority of flexible circuits. When designing a flexible circuit, the minimum conductor thickness and width should be determined on the basis of current carrying capacity and the maximum permissible conductor temperature rise. Since the conductors in a flexible circuit are both thin and flat, they provide about 50% more surface area than a round wire of equivalent cross section. This allows for more efficient dissipation of heat. Therefore, a flexible conductor can carry more current at a reduced size when compared to round conductors; it may be possible to uprate the AWG requirements by one or two gage sizes.

To determine the conductor width necessary for a given current or resistance, a conductor nomograph can be used. The nomograph in Figure 4-1 shows the current carrying capacity for a given conductor width and thickness which will yield a 10°C temperature rise at 20°C ambient. The temperature rise of 10°C is the standard used in flexible circuit boards.

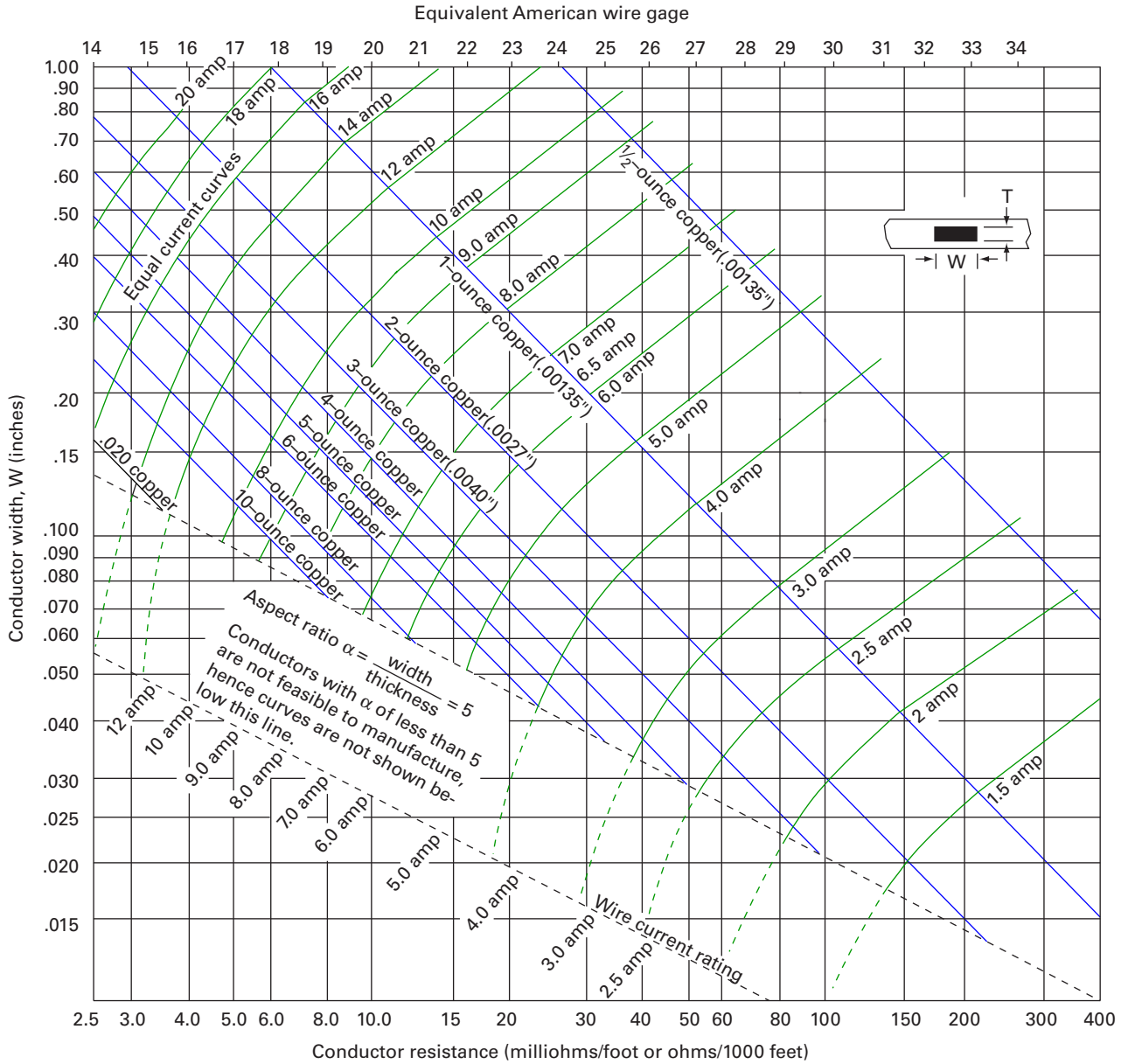
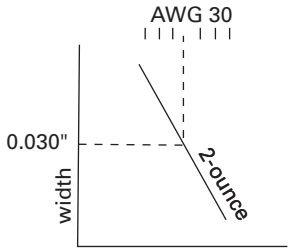


Figure 4-1. Conductor Resistance Nomograph.

THE BASICS

NOMOGRAPH USE EXAMPLES

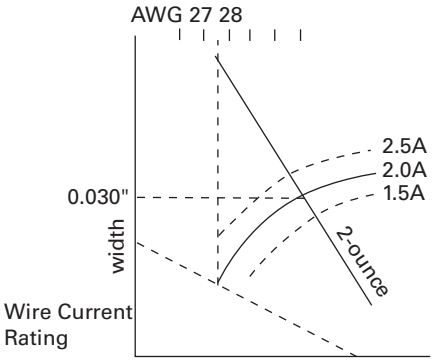
1) Find the AWG round wire size with the equivalent resistance rating of a 2 oz. X 0.030" conductor:



From 0.030" on the width scale, project horizontally to the 2 oz. curve.

Project vertically to the AWG baseline and read 30 as the closest AWG wire size.

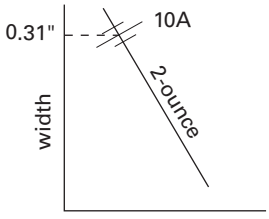
2) Find the AWG wire size that can carry a current equal to a 2 oz. X 0.030" conductor.



From the 0.030" on the width scale, project horizontally to the 2 oz. line. The intersection occurs at the 2A constant current curve.

Follow that curve down to the intersection with the Wire Current Rating line. Project that intersection vertically to the AWG baseline and read 28 as the closest AWG wire size.

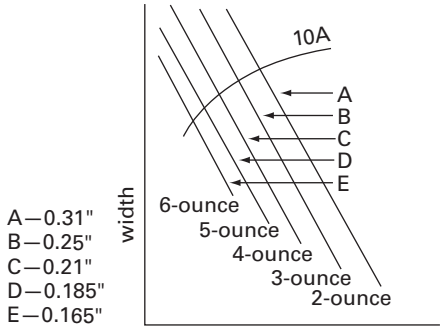
3) Find the width of a 2 oz. flat conductor that can safely carry 10A without exceeding a 10°C temperature rise.



a) Locate the intersection of the 2 oz. line with the 10A constant current curve.

b) Project that intersection horizontally to the width scale and read 0.31".

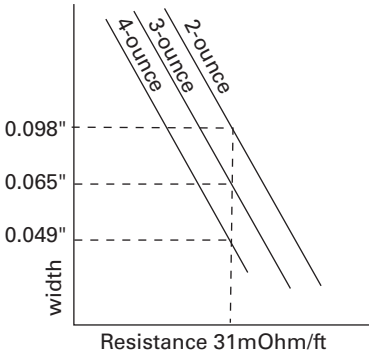
4) Find other combinations of width and thickness for conductors capable of carrying 10A without exceeding a 10°C temperature rise.



a) Note the intersection on the 10A constant current curve with 3, 4, 5 and 6 oz.

b) Project each horizontally to the width scale and read 0.25", 0.21", 0.185" and 0.165".

5) Find the flat conductor size for handling 4A at a maximum drop of 0.125V/ft.



a) Calculate the required resistance per foot from R = E/I = 0.125/4 = 0.031 Ohm/ft = 31 mOhm/ft.

b) Locate this resistance on the baseline and project it vertically to intersect the 2, 3 and 4 oz. lines.

c) Project these intersections horizontally to the width scale and read 0.098", 0.065" and 0.049".

d) If selecting the conductor on the basis of the lowest temperature rise, choose the 2 oz. X 0.098" size; it has about 100% more surface area than the 4 oz. conductor and about 33% more surface area than the 3 oz. conductor.

Conductor Spacing

The clearance between two conductors on individual layers, or from a conductor to the edge of an assembly, is determined, in part, by the voltage requirements of the conductors. Figure 4-1 shows the minimum spacing requirements for various voltage ratings. It should be noted that these are minimums and that the artwork must be designed with these requirements in mind. The use of a covercoat insulation material will enhance the electrical performance for clearance requirements, as there will be no ionization of the air surrounding the conductors resulting in flashover. Often, the spacing on a flexible circuit is chosen more by manufacturing considerations than by electrical performance requirements, since the operating voltages for most flexible circuit designs are relatively low. In addition, the insulating materials used can withstand 300 V/mil or more.

Temperature Rise vs. Current

The chart shown in Figure 4-2 has been prepared to estimate temperature rises above ambient versus current for various cross-sectional areas of etched copper conductors. A 20% derating for unknown variations should be included. An additional 15% derating is suggested for conductor thicknesses of 0.0042 inch (3 oz/ft2) or more.

CONDUCTOR SPACING CONSIDERATIONS

VOLTAGE	COVER-LAYERED BOARDS ANY LEVEL	UNCOATED BOARDS < 10K FT. Altitude	UNCOATED BOARDS > 10K FT. Altitude
0-50	0.005"	0.025"	0.025"
51-100	0.005"	0.025"	0.060"
101-150	0.016"	0.025"	0.125"
151-250	0.016"	0.050"	0.125"
251-500	0.030"	0.100"	0.250"
> 500	0.00012" per volt	0.0002" per volt	0.001" per volt

Table 4-1.

Permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate, and the maximum ambient temperature in the location where the panel will be used. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness,

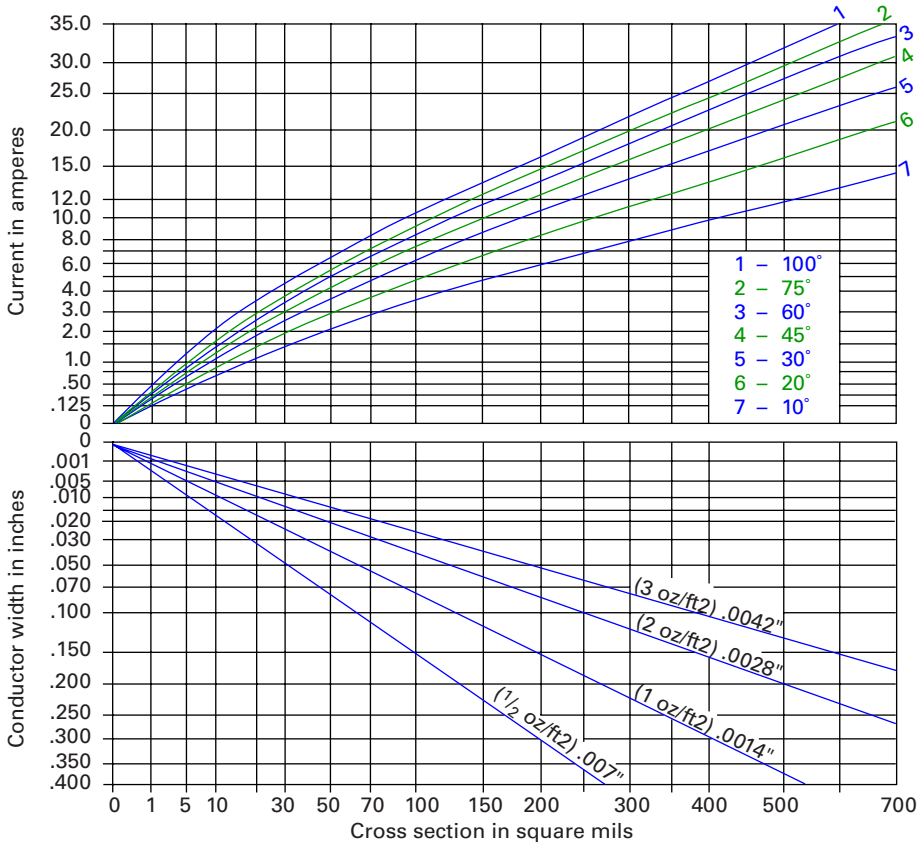


Figure 4-2. Chart to be used to determine current capacity and sizes of etched copper conductors for various temperature rises above ambient.

cross-sectional area, and current-carrying capacity for various temperature rises. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of cross-sections of the parallel conductors. The equivalent current is the sum of the currents in the conductors. The effect of heating caused by the attachment of power dissipating components is not included.

Shielding

Many applications for flexible circuitry require shielding of certain conductors to prevent cross-talk or for other electrical considerations. Certain shielding requirements can be avoided by carefully laying out the artwork. Care should be taken to locate sensitive conductors away from radiating lines to avoid cross-talk, with less critical conductors in between, if necessary. Grounded guard connectors can also be placed next to the sensitive conductors to help isolate them from interference.

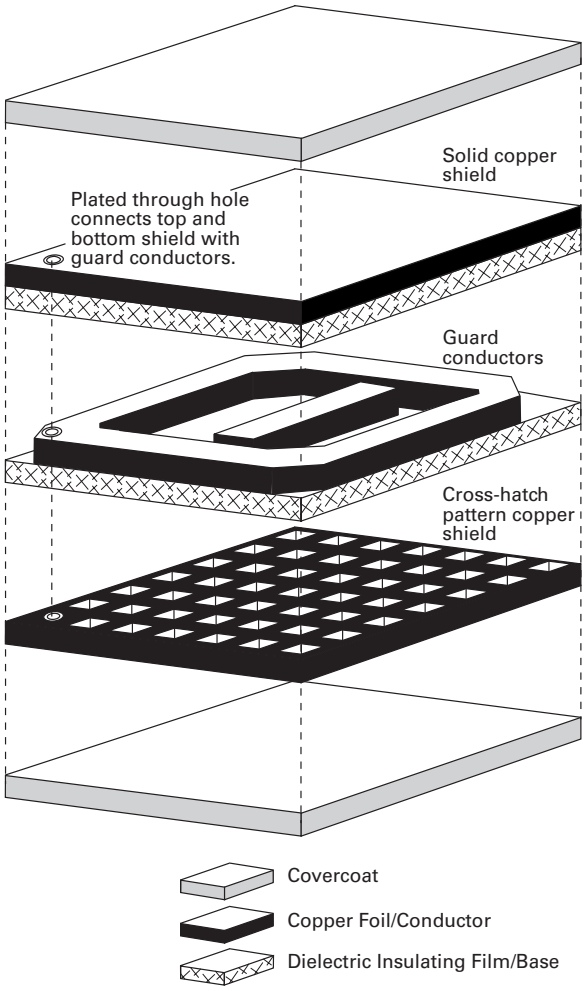


Figure 4-3. Shielding Techniques.

When full shielding is required, it can be accomplished by using either thin copper foil, or a screened-on silver epoxy compound, along with guard conductors for a full circumferential shield. Thin copper foil is the most cost-effective method while still maintaining flexibility; when used, it is necessary to use a cross-etch pattern to provide improved flexibility and bond strength to the base dielectric. The thin foil can also be tied into guard conductors via plated-through holes for full circumferential shielding.

Dielectric Properties

There are a variety of thin film dielectric materials that are available for use in flexible circuitry. These materials have differing dielectric properties which may significantly effect the electrical design. Table 4-2 lists the dielectric values for some of the high-temperature thin film dielectrics. These values should be used in calculations requiring dielectric constant or strength values. Where combinations of dielectrics are used, their dielectric constants based on the percentage of each material can be calculated from the following formula:

$$D_{K_{EFFECTIVE}} = \frac{A}{\frac{B}{C} + \frac{D}{E}}$$

Whereas:

A = Overall thickness of both materials

B = Overall thickness of 1st material

C = Dielectric constant of 1st material

D = Overall thickness of 2nd material

E = Dielectric constant of 2nd material

Characteristic Impedance

Most often associated with a transmission line, characteristic impedance is the single most important electrical property used to determine the performance of a high-speed circuit. A transmission line is defined as one signal-carrying circuit composed of conductors and dielectric insulating material, with highly controlled physical and electrical parameters, used to carry high frequency or narrow pulse-type signals.

There are two general configurations of transmission lines which can be used during the design to better achieve controlled impedance in a flexible circuit. The first type is the micro-strip configuration, in which the conductor is located above a single ground plane. The second type is the stripline configuration, in which the

DIELECTRIC STRENGTH AND CONSTANT

MATERIAL	STRENGTH V/0.001" (25µm)	CONSTANT 1 MHz
Polyimide Film w/ Acrylic Adh.	4,500	3.8
Adhesiveless Polyimide Film	6,000	3.2
Acrylic Adhesive	1,900	4.0
Epoxy Glass Prepreg	1,131	4.3
Polyimide Glass Prepreg	1,330	4.3
Teflon Film	5,000	2.1

Table 4-2.

conductor is centrally located between two ground planes. In either construction technique the characteristic impedance is dependent on the conductor width and thickness, the dielectric thickness, and the dielectric constant of the insulating material. If the impedance (Zo) is controlled, then any mismatch or signal reflection which results from the passage of fast pulses through an impedance discontinuity will be avoided.

Teledyne's design engineers have developed sophisticated software programs that calculate the impedance value for specific design criteria. The programs can be manipulated to solve for either the design requirements (e.g. conductor width, shield spacing, etc.) or the material selection required to meet a desired impedance value.

The chart in Figure 4-4 shows the relationship between impedance and the distance required between ground planes along with the appropriate conductor width. If the desired characteristic impedance value of the circuit is known, then the distance between ground planes (dielectric thickness) and conductor width can be found relatively quickly. In this chart, the curves plot the impedance in relationship to the dielectric constant of the insulating material by using the expression:

$$\sqrt{\langle \varepsilon r \rangle}\ Z_o$$

An example of using this chart follows:

A circuit design requires a characteristic impedance value of 50Ω minimum. The dielectric insulating material is polyimide film coated with acrylic adhesive (εr = 3.3 @ 1 MHz).

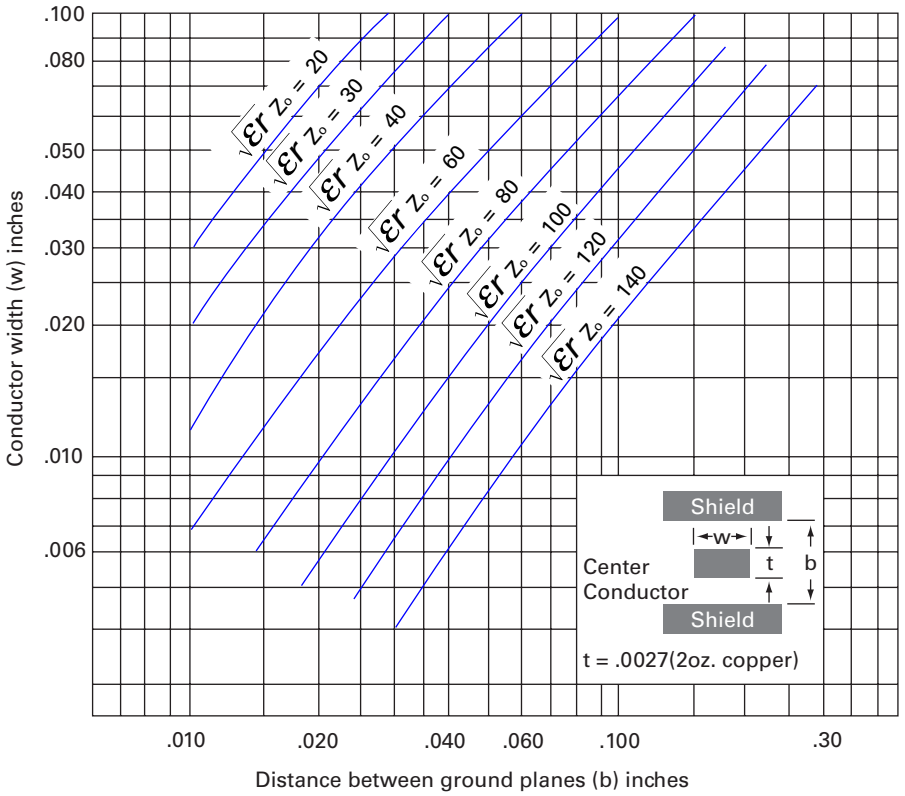


Figure 4-4. Characteristic Impedance (Z_o) normalized curves.

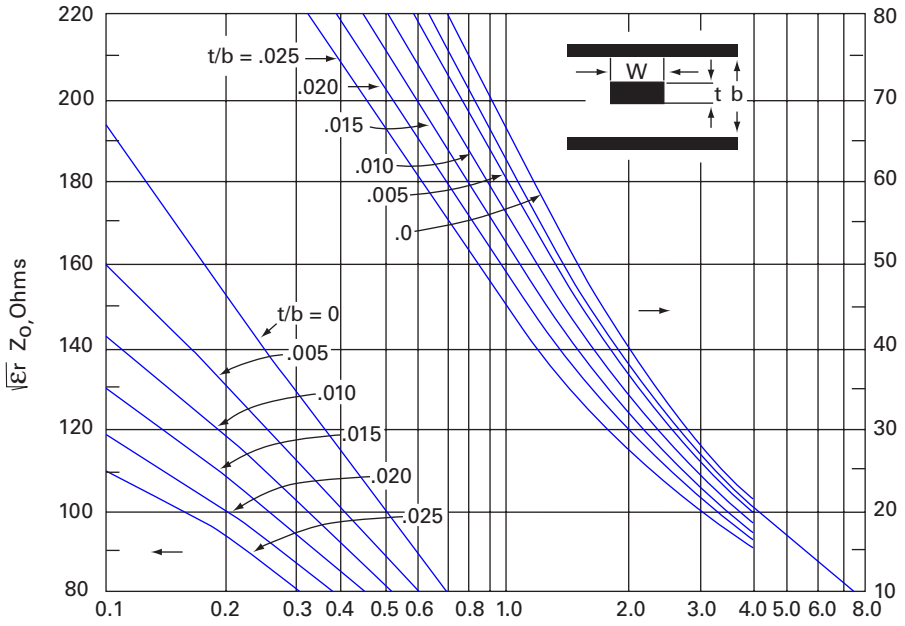


Figure 4-5. Graph of Z_o versus w/b for various values of t/b.

$\sqrt{\langle \varepsilon r \rangle}\ Z_o$ = Normalized curve

εr(polyimide film) = 3.3

Z_o = 50 Ohms

$\sqrt{3.3}$ = 1.82

Then 1.82 x 50 = 91 (curve)

For a conductor width of

0.020", b = .046

0.010", b = .028

0.008", b = .021

From the example shown, it becomes apparent that an increase in the conductor width has a corresponding influence on the overall thickness of the circuit, which in turn affects the flexibility. Similarly, selecting a material with a lower dielectric constant allows a reduced overall thickness.

Calculations

High Frequency Lines

The general calculation for characteristic impedance for any high frequency transmission line is:

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

where

Z_o = impedance, Ω

R = resistance per unit length of line

L = inductance per unit length of line

G = conductance per unit length of line

$\omega = 2\pi f$

C = capacitance per unit length of line

If the line is lossless, the equation can be simplified to:

$$Z_o = \sqrt{\frac{L}{C}}$$

Micro-Strip

The specific formula for a microstrip configuration is:

$$Z_o = \frac{h}{w}\frac{377}{\varepsilon r}$$

h = thickness of the dielectric

w = width of the conductor

εr = the effective dielectric constant of the insulating material (considering the effect of air.)

If the micro-strip line is also covercoated, the characteristic impedance values obtained by using this formula will be reduced by approximately 20 percent. This formula disregards the fringing effects and any leakage of a micro-strip transmission line. To accurately account for these factors the following formula is recommended:

$$Z_o = \frac{h}{w}\frac{377}{\sqrt{\varepsilon r}\cdot\{1 + (2h/(\pi\omega))[1 + \ln((\pi\omega)/h)]\}}$$

Stripline

The characteristic impedance of a stripline configuration can be calculated using the following equation:

$$Z_o = (60/(\sqrt{\varepsilon r}))[\ln(4b/d_o)]$$

where d_o, the effective wire diameter for a square configuration, is 0.567w + 0.67t.

Because this equation is cumbersome, the family of curves shown in Figure 4-5 has proven to be very useful in determining stripline parameters. They are applicable to the multiple variations in dielectric thickness to conductor widths in a stripline configuration.

Notes

1. Impedance calculations should be considered as rough estimates for constructions. The formulae actually used take into consideration empirically determined factors which are process-specific.
2. Ground shields need to be in intimate contact with signal flex legs to provide true impedance control.

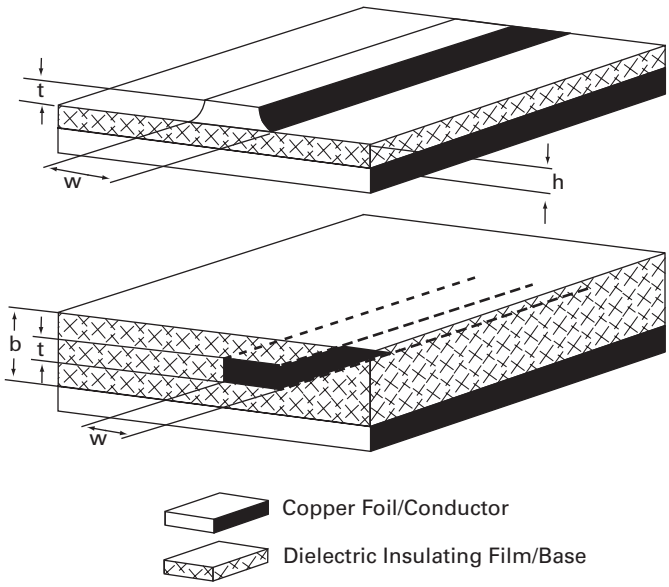


Figure 4-6. Printed wiring transmission line configurations.

Distributed Capacitance

Capacitance is the property of an electric non-conductor that permits the storage of energy. In flexible circuitry the capacitance between adjacent conductors consists of both parallel-plate capacitance (Cp) and fringing capacitance (Cf). The distributed capacitance (Cd) is the sum of Cp and Cf. Since the conductors are very thin, and thus have small areas exposed to each other, the parallel-plate capacitance is generally negligible. Therefore, we will first discuss the effects of fringing capacitance (Cf) on flexible circuit performance.

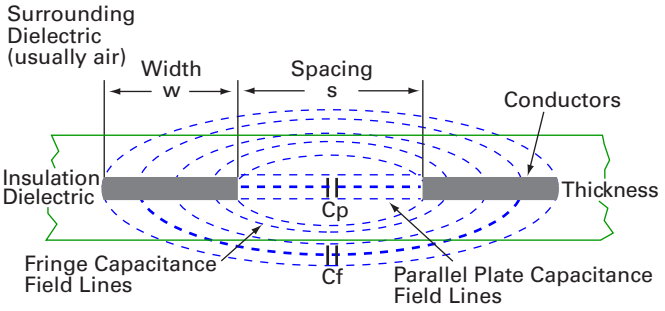


Figure 4-7. Distributed capacitance between conductors is the sum of the parallel plate (Cp) and fringing (Cf) capacitances.

The fringing capacitance value in a flexible circuit is dependent on:

- the thickness and dielectric constant of the insulating material
- the width and thickness of the conductors
- the spacing between the conductors

Other factors that affect capacitance are the close proximity of the signal to ground, and the frequency of the signals. Since some portion of the fringing field extends into the air outside the insulation, it is necessary to establish a “median” value for the dielectric constant which falls between that of the air and that of the insulating material. This median value of the dielectric constant would then be used in any calculations. The capacitance values calculated using this approximation will then serve as a guideline of what the actual distributive capacitance will be for a given circuit configuration. Actual measurements are required to obtain accurate capacitance values for high frequency circuits. This is due, in part, to the effect of the above factors, and variation of dielectric constants of the materials with frequency.

The results of a sample calculation are shown in Figure 4-8. This graph shows the calculated capacitance

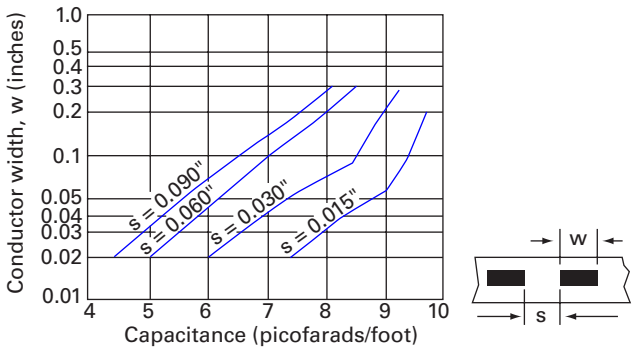


Figure 4-8. Calculated capacitance between two adjacent parallel conductors.

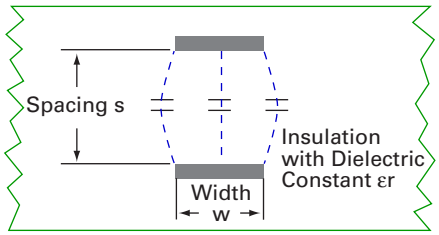


Figure 4-9. Capacitance between two conductors with large surfaces is largely parallel-plate capacitance, Cp.

between two adjacent parallel conductors insulated using 0.005" of polyester. To determine the distributed capacitance for a flexible circuit using a different dielectric material, simply multiply the value shown in this graph by the proper dielectric constant ratio for the desired insulating film. For applications in which the conductors are completely enclosed by the insulation and have surfaces facing each other, it may be necessary to calculate the capacitance between the conductors. This is especially true for designs involving high frequencies. An example of this type of configuration is shown in Figure 4-9.

To find the capacitance for conductors with other insulation materials, multiply the results found above by the ratio of constants shown in Table 4-3.

RATIO OF DIELECTRIC CONSTANTS

Polyester	1.0
FEP Teflon	0.90
Polyimide	1.3

Table 4-3.

The formulas for these calculations are shown below in the following relations:

For $\frac{w}{s} < 1$

$$C_{Total} = \frac{3.68\ \varepsilon r}{\log_{10}\left[\frac{4s}{w}\right]}\ pF/ft.$$

When using this calculation, the result will be approximately 2% high for W/S < ½ and approximately 10% high for W/S = 1.

For $\frac{w}{s} > 1$

$$C_{Total} = 2.7\frac{w}{s}\varepsilon r \cdot \left[1 + \frac{s}{\pi w}\left(1 + 2.303\log_{10}\frac{2\pi w}{s}\right)\right] pF/ft.$$

When using this calculation, the result will be approximately 4% low for W/S = 2 and approximately 10% low for W/S = 1.

For the above formulas:

w = width of conductor, ft.

s = dielectric separation between conductors, ft.

C_{Total} = capacitance, pF/ft.

εr = dielectric constant of insulating film

Capacitance for flat etched conductors to surrounding metallic shields and/or ground planes is shown in Figure 4-10 for standard flexible wiring using FEP Teflon® insulation.

To help reduce the effect of distributed capacitance on an etched conductor, it is necessary to add grounded guard conductors. These guard conductors will cause some of the fringe flux lines to terminate, and therefore, will not contribute to the measured value. Examples can be found in Figure 4-11. Measurements made between two conductors guarded by two grounded conductors will show about a 20% reduction in capacitance as compared to unguarded conductors. Capacitance between two conductors can be even more dramatically reduced (> 80%) when a grounded guard conductor is placed between them and a grounded conductor is placed on either side.

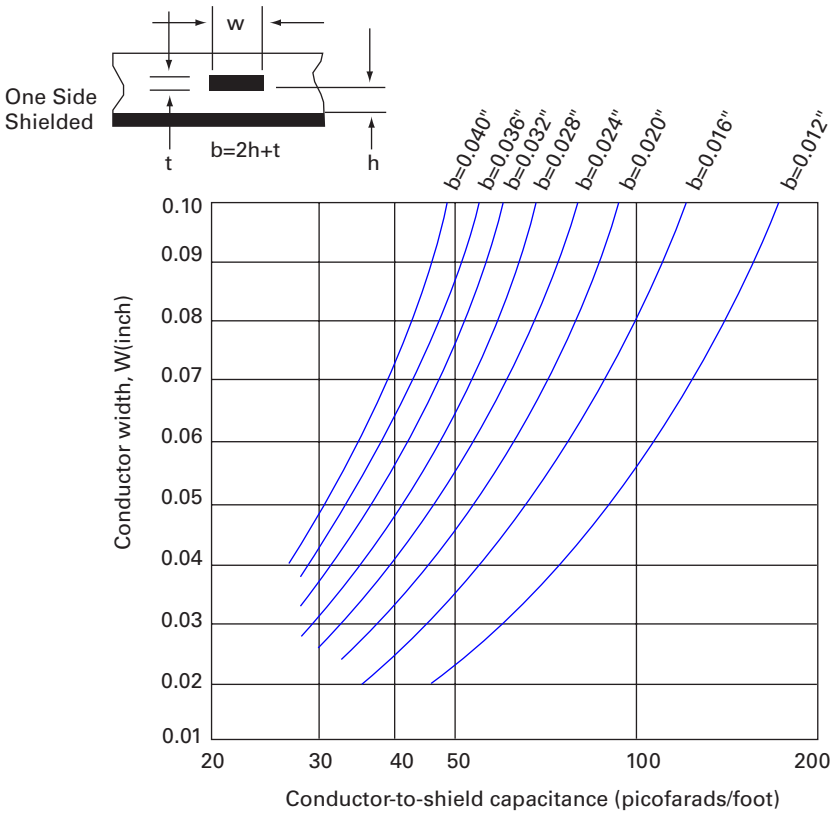


Figure 4-10. Typical conductor-to-shield capacitance for 2-oz. copper conductors insulated with FEP Teflon®.

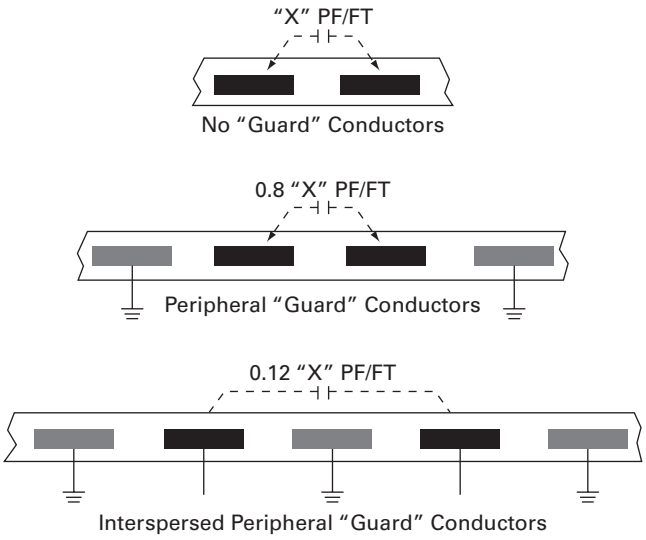


Figure 4-11. Conductor "guarding" by adjacent grounded conductors.

5

Mechanical Design

Chapter Terms

Bookbinder Effect: A manufacturing technique in which the circuit layers are manufactured with progressive lengths in the flexible section. This allows the flexible circuit to be tightly bent in limited space without delamination.

Conformal Coating: An insulating protective covering that conforms to the configuration of the objects coated when it is applied to a completed printed board assembly.

Covercoat or Cover Lay: The layer of insulating material that is applied over a conductive pattern on the outer surface of a printed circuit. Used for electrical insulation and environmental sealing.

Fiducial Mark: A printed board artwork feature (or features) that is created in the same process as the printed board conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern or land patterns.

Global Fiducials: Fiducial marks that are used to locate the position of all of the land patterns on a printed board.

Hold Down Tabs: Conductive tabs extending from the outside of an annular ring or other termination pad used to help secure the pad to the substrate.

Plated-Through Holes: A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board.

Polyimide: A dielectric film material commonly used for flexible circuit fabrication as an insulating layer.

Terminal Pad: A portion of a conductive pattern that is usually used for making electrical connections, for component attachment, or both.

Unsupported Hole: A hole that does not required plating-through. Most often found in single- and double-sided circuits.

Vias: A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material.

In addition to providing highly reliable and repeatable electrical interconnection performance, flexible circuitry can significantly improve the electronic package by reducing both size and weight, and improving its appearance. This section covers the mechanical design features that should be considered to fully utilize the benefits of this technology.

Folding and Bending

One of the inherent characteristics of flexible circuitry is its ability to be flexed and bent during installation and use. To facilitate bending, care must be taken during the design stage to ensure proper material selection and conductor placement. The formability of the flexible circuit is dependent on both the insulating material used, and to a certain degree, on the thickness and the ductility of the copper.

Terminal areas on a single-sided circuit can be designed to allow for double access of the circuit by folding the circuit. This method is more cost-effective than using a double access (reverse bared) circuit or a double-sided circuit. The circuit can be formed using three methods — cold forming, thermoforming, or reinforced forming in which the copper weight and/or conductor widths are used to assist the circuit in maintaining a fold. The folded portions of a circuit may be secured with either a heat-activated adhesive, or a pressure-sensitive bonding agent. When choosing any one of these three methods, it is advisable to use a small rod or wire mandrel to help control the bend radius and to prevent the conductors from becoming damaged during the forming operation. Preheating the circuits to 65-125°C will also assist in forming them.

Continuous Flexing

For any circuit that is required to operate in a continuous flexing mode, it is important that the manufacturer be consulted regarding insulating material selection to ensure the unit will have the necessary mechanical and electrical properties. The construction must allow the copper to be in the neutral axis (centered between the dielectric materials). The design should also specify the use of the softer and more ductile rolled annealed coppers, rather than electro-deposited, to prevent failures caused by metal fatigue. Depending on the conductor layout, material selection, electrical conditions, the environment to which the circuit will be exposed, and the bending modes, flexible circuitry can provide over 500,000 flex cycles before failure.

Bend Radii

Bend radii should always be kept as large as possible to prevent damage to the circuitry. Refer to Table 5-1. For military applications the minimum allowable bend radius should be six (6) times the maximum overall thickness for one and two conductor layer flexible products. An example of a one conductor layer flexible product would be approximately 0.005" to 0.007" (125µm to 175µm) thick. Multiply the average thickness of 0.006" (150µm) by 6X and the minimum allowable bend radius would be from 0.030" to 0.042" (0.75mm to 1.06mm). A two conductor layer circuit would be approximately 0.012" to 0.0150" (300µm to 380µm), or a bend radius of 0.072" to 0.090" (1.82mm to 2.25mm).

A Type 3 multilayer circuit is a circuit with more than 2 layers (usually products run from 3 to no more than 12 layers) with plated through holes. These circuits have no rigid laminate to rigidize the connector patterns and have all the layers laminated together. This type of circuit would measure from 0.015" (380µm) to approximately 0.062" (1.57mm) thick. The minimum bend radius of a Type 3 circuit is twenty-four (24) times the overall laminate thickness or 0.360" (914µm) to approximately 1.5" (38.1mm) bend radius.

A Type 4 circuit or otherwise known as a Rigid Flex Circuit could be designed with a minimum of 3 layers to an amount only limited by the manufactures capabilities, usually about 25 to 30 layers. These circuits would be made up of single- or double-sided flex layers which would not be bonded together. This allows maximum

BEND RADII

Circuit Type	Bend Radii	
	Commercia	Military
1-Single-sided	1x	6x
2-Double-sided; plated through holes	4x	6x
3-Multi-layer, flexible; plated through holes	24x	24x
4-Single-sided; unbonded Double-sided, unbonded	5x 7x	12x 12x
5-Multi-layer; no plated through holes	12x	12x

[1] Commercial - flex to install

[2] Military - no electrical or mechanical damage after 25 flex cycles

Table 5-1.

flexibility. This type of circuit it is recommended to use a bend radius of twelve (12) times the overall flexible thickness cross-section.

TYPICAL MATERIAL THICKNESS

COPPER

Weight	Thickness	
1/2 ounce	0.0007"	17µm
1 ounce	0.0014"	35µm
2 ounce	0.0028"	70µm
3 ounce	0.0042"	105µm

EPOXY PREPREGS

Glass Style	Thickness (after lamination)	
106	0.0015" ± 10%	35µm
1080	0.0028" ± 10%	70µm

DIELECTRIC MATERIALS

Film Thickness	Adhesive Thickness	Laminate Thickness	
Polyimide Film as Base Laminate on Single-Sided Circuitry or Innerlayer			
1 mil	adhesiveless	0.001"	25µm
1 mil	1 mil/one side	0.002"	50µm
2 mil	1 mil/one side	0.003"	75µm
Polyimide Film as Base Laminate on Double-Sided Circuitry or Innerlayer			
1 mil	adhesiveless	0.001"	25µm
1 mil	1 mil/two side	0.003"	75µm
2 mil	1 mil/two side	0.004"	100µm
Polyimide Film as Covercoat			
1 mil	1 mil/one side	0.002"	50µm
2 mil	1 mil/one side	0.003"	75µm
1/2 mil	1 mil/one side	0.0015"	35µm
1 mil	1 mil/one side	0.003"	75µm
2 mil	1 mil/one side	0.004"	100µm

Table 5-2.

Flex Section Length

For multi-layer rigid-flex the designer must calculate the overall length of the flexible section to assure that it will be long enough to allow the circuit to fold into the intended shape without putting unnecessary stress on the materials. The formula used to calculate the flex length takes into account the bend radius required as outlined in the previous section *Bend Radii*. Please refer to this section for direction on how to calculate the bend radii for your application.

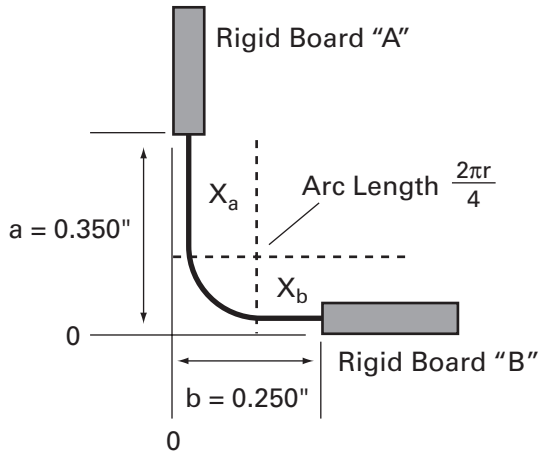


Figure 5-1. Factors to consider when calculating flex length for a 90° to 135° bend.

To Calculate Flex Length For 90° Bend

The formula used to calculate flex length for a 90° bend (and up to 135°) is as follows:

$$F.L. = \frac{2\pi r}{4} + (X_a + X_b)$$

where:

F.L. = Flex Length

$\frac{2\pi r}{4}$ = Arc Length

r = radius, which must be equal to 12 x t, where t = flex thickness

X_a = a-r and

X_b = b-r

The following is an example of this equation for the lay-out shown in Figure 5-1. In this example:

a = 0.350"
b = 0.250"
t = 0.010"

First calculate for r:

r = 12 x t where t = .010

r = 12 x .010 = 0.120"

Next calculate X_a:

$X_a = a\text{-}r$

$X_a = .350 - .120 = 0.230"$

Next calculate X_b:

$X_b = b - r$

$X_b = .250 - .120 = 0.130"$

Note: Value for either a or b must always be larger than value for r.

To calculate the flex length using the formula:

$$F.L. = \frac{2\pi r}{4} + (X_a + X_b)$$

$$F.L. = \frac{2\pi r(.120)}{4} + (.230 + .130)$$

F.L. = 0.548"

Rounded to the nearest 2 place decimal:

F.L. = 0.55"

Note: The overall flex length must always be larger than $a^2 + b^2 = c^2$ and less than a + b.

In our example the flex length equaled 0.55".

Therefore:

$a^2 + b^2 = c^2$

$.350^2 + .250^2 = c^2$

$.1225 + .0625 = c^2 = .185$

$c = \sqrt{.185} = 0.430"$

and

a + b = .350 + .250 = 0.600"

Therefore:

$a^2 + b^2 = c^2 <$ F.L. < a + b

0.430" < 0.550" < 0.600"

To Calculate Flex Length For 180° Bend

To calculate a correct fit and flex length for rigid-flex circuits that will be bent 180° the physical constraints of the unit must be known prior to calculating flex length. The distance between the boards when folded, which is the maximum bend radius, must be taken into account. Also, the distance to any wall or obstruction in the flex area must be known so that the flex section will not be too long. Refer to Figure 5-2.

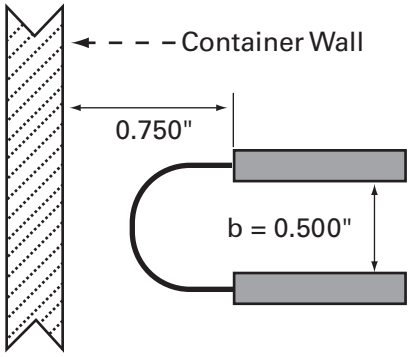


Figure 5-2. Constraints to consider for flex length for a 135° to 180° bend.

The formula used to calculate flex length for bend angles greater than 135° and up to 180°, is:

$$F.L. = \frac{2\pi r}{2}$$

In this equation r is the radius found when measuring the desired distance between the boards (B dimension in Figure 5-2.

r = B ÷ 2

The minimum bend radius, based on the thickness of the flexible section, must still be considered. The calculation is:

r = 12 x t

Refer to the section of this chapter titled *Bend Radii* for additional information on calculating minimum bend radii.

To calculate the flex length for the circuit shown in Figure 5-2 the following values would apply:

B = 0.500" (distance between the boards)

r = B ÷ 2

.500 ÷ 2 = 0.250"

The calculated flex length would then be:

$$F.L. = \frac{2\pi r}{2}$$

$$F.L. = \frac{2\pi(.250)}{2} = 0.785"$$

For extremely tight bends in a limited space, rigid-flex manufacturers can produce circuits in which the circuit layers are manufactured with progressive lengths in the flexible section allowing for a “bookbinder” type effect when folded. This type of design requires compensation

during the design and manufacturing processes, resulting in a premium price.

Fold Areas

The areas on a flexible circuit that are to be bent or folded must be designed in a way that accommodates this type of application. The conductors should always be laid out perpendicular to the fold line as shown in Figure 5-3. Plated-through holes, component holes, surface mount terminal pads, and mounting holes must be located a minimum of 0.100" (2.54mm) away from the fold area.

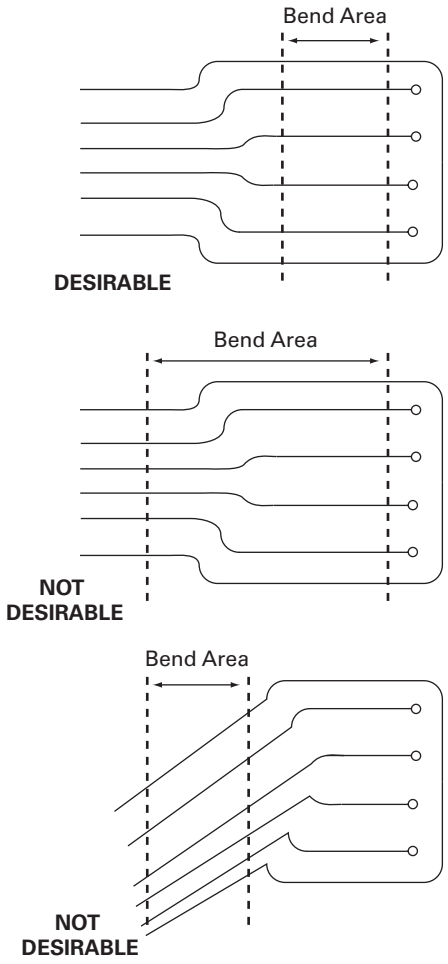


Figure 5-3. Conductors should always be designed at right angles to the fold line.

Another consideration when designing a circuit for a folding application is the relative relationship of the volume of copper to the flexible dielectric. A circuit with excessive edge distance in the fold area can cause folding problems, due in part to the memory characteristic of the flexible laminate. In these areas it is advisable that the edge clearance be greater than 0.020" (500µm), but should not exceed 0.100"(2.54mm).

For circuits in which bend strengthening is necessary or where cold forming is required, it will be necessary to increase the ratio of copper to flexible dielectric. Copper strips of various lengths can be built into the circuit as shown in Figure 5-4 to strengthen selective areas.

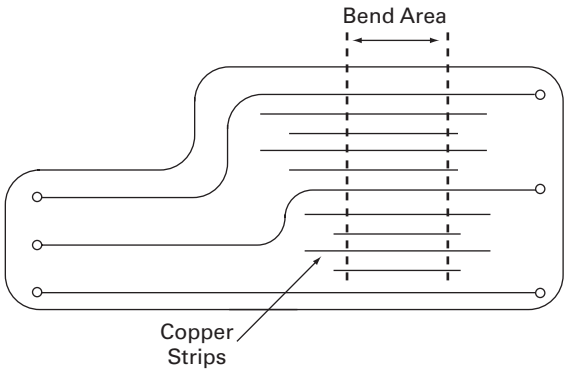


Figure 5-4. Strengthened techniques.

Tear Stops

The addition of tear stops is strongly recommended where sharp interior corners must be used. There are several ways to incorporate tear stops into the design of flexible circuits. One way is to supply a copper dam on the artwork that will reinforce an interior angle. Another is to supply glass-cloth or polyimide stiffeners to all inside radii. These stiffeners can be heat laminated to the circuitry when the covercoat is bonded and they will provide the additional notch strength required. Of the two methods, the glass-cloth or polyimide stiffener is preferred. This method provides the needed support to prevent a tear, whereas copper reinforcement only helps stop a tear from propagating. The additional copper also must be part of the etched pattern and could affect the layout of the conductive pattern. In applications requiring a slit, the design should incorporate a tear stop at the end of the slit.

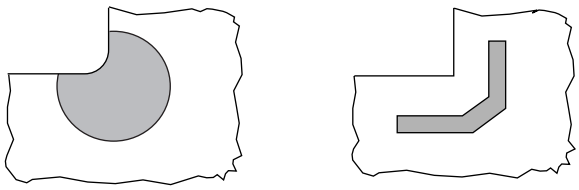


Figure 5-5. Tear stops.

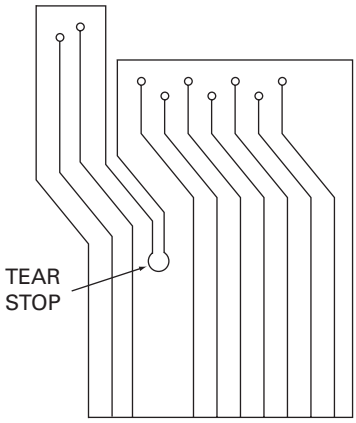


Figure 5-6. Tear stops at the end of slits are needed to protect the circuit.

Terminal Baring

There are a variety of methods available to remove the covercoat insulating material above the terminal pads to electrically expose them. These methods are normally used on single layer and double layer circuits that employ covercoats. For multi-layer applications, the most cost-effective way to gain pad exposure is to add a pads-only layer to the artwork. This additional layer provides sufficient copper for through hole plating while excluding the costly operations of adding predrilled covercoats to the multi-layer circuit. Because all copper outside of the pad areas is etched away, there is no plated copper on the conductors, resulting in greater flexibility. Figure 5-7 shows three of the most common terminal baring techniques used in flexible circuits.

The individual baring method is preferred for military applications. Using this method, the covercoat insulating material is either pre-drilled or pre-punched prior to covercoat lamination to allow access to the termination areas. Notice that the pads incorporate hold down tabs which are encapsulated by the covercoat. These tabs help prevent the pads from lifting from the base dielectric during soldering operations. Without them, the covercoat opening must be reduced for a 360° 0.010" (250µm) overlap of the pad, reducing the solderable area.

The slot method is used to bare more than one termination pad per opening. Because of the increased tooling cost to punch an irregular shape, this method should be used only as a last resort or when there are high production volumes. Laser isolation is an alternative for small volumes or irregular shapes.

With the strip method, multiple termination pads can be bared at one time using a variety of manufacturing techniques. This method has found widespread acceptance in commercial applications because of its cost-effectiveness.

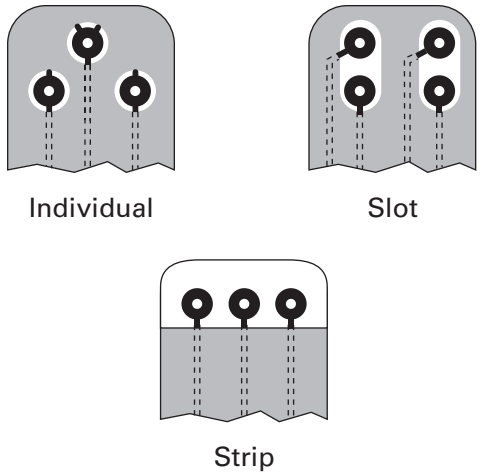


Figure 5-7. Three methods for baring conductor terminals in flex circuits.

Circuit Periphery

The shape of a flexible circuit should be as simple as possible. Sharp internal corners should be avoided. All internal radii should be reinforced with tear stops. All corners should be chamfered or have a radius of at least 0.015" (375µm). Edge distance tolerances should be as loose as possible without affecting space requirements for electrical insulation. Avoid tolerances tighter than 0.010" (250µm).

Shock and Vibration Considerations

When a flexible circuit is to be subjected to a shock or vibration environment, special attention must be placed on the components and their placement, as well as the proper securing of the circuit itself. The components that will be mounted on the board should be lightweight, low profile components, with inherent strain relief. Components having irregular shapes, especially those having a large mass and a high center of gravity, should be avoided. If these types of components must be used,

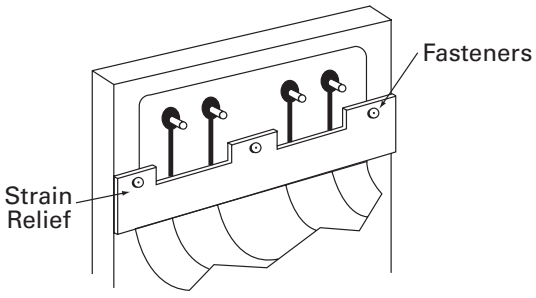


Figure 5-8. Strain bars, screws or clips can be used for circuit mounting.

they should be placed in a rigidized section of the circuit where proper fastening can be achieved. Proper attention must be paid to workmanship during assembly and handling to assure that the component leads are properly bent and not nicked. Components should always be mounted in such a way as to minimize movement. For axial leaded components weighing more than 0.25 ounce (7 grams) that are impractical to clamp, proper mechanical strengthening can be accomplished by encapsulating the leads using an epoxy based adhesive material. This method will provide mechanical support and will isolate the solder joints from the environment.

To reduce the effects of shock and vibration on the circuit itself, it is necessary to provide support to both the rigidized and flexible sections. Mounting can be accomplished by providing mounting holes as part of the periphery of the circuit, as shown in Figure 5-9. Mounting hardware such as screws, strain bars or clips can be used in conjunction with these mounting holes for properly securing the flexible circuit.

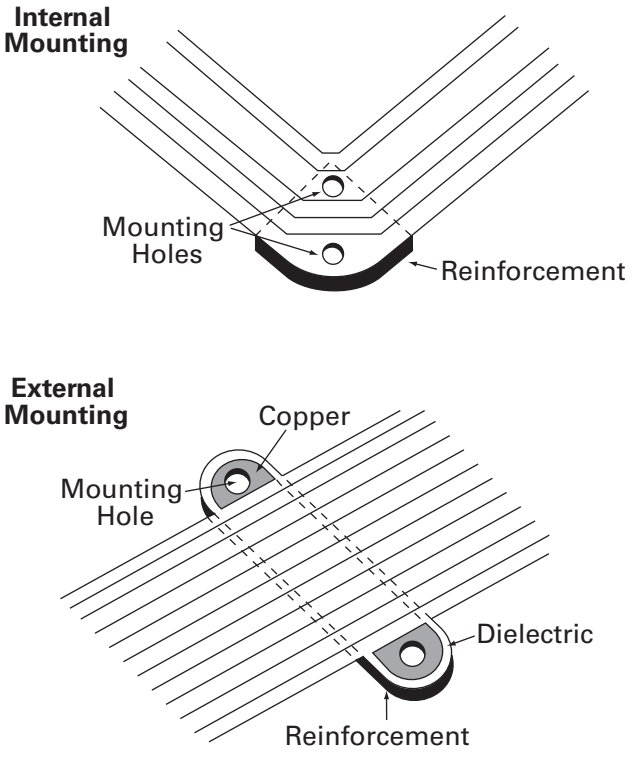


Figure 5-9. Mounting holes can be built in, internally or externally, to secure circuits.

Rigid Reinforcement

Single-sided and double-sided flexible circuits can be stiffened in certain areas by the addition of a rigid reinforcement material. This provides areas for component mounting, as well as additional mechanical strength and

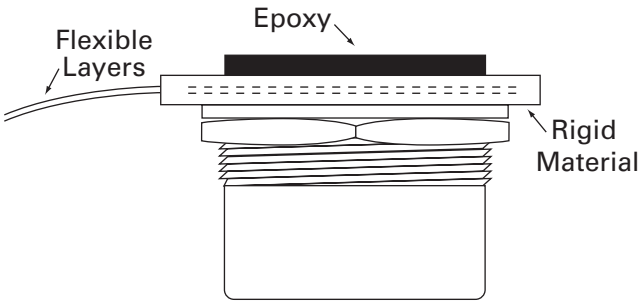


Figure 5-10. Terminal areas can be potted for strain relief and environmental protection.

stiffness. Common reinforcement materials are 0.005" (125µm) or thicker polyimide films and epoxy glass; less common materials are polyester film, sheet metal and phenolics. These stiffeners are normally bonded to the flexible circuit with an adhesive similar to that used in the construction of the flexible circuit itself. Alternative adhesives such as heat-activated or pressure-sensitive adhesives can be used depending on the particular application. With heat-activated adhesives, the curing regime must be carefully controlled. Once the stiffeners are bonded to the flexible circuit, rework of the assembly can become an issue.

Holes drilled in the stiffener material should be drilled a minimum of 0.014" (350µm) larger in diameter that the corresponding holes in the flexible circuit. This oversizing of the hole diameters will allow for any misregistration of the stiffener to the pads on the circuitry. When an epoxy glass material is used as a stiffener, it is beneficial to add a bead of strain relief to provide a radius between the rigid material and the flexible circuit. This assists in the transition from the rigid to the flexible sections and prevents damage during flexing operations.

Tolerances

There are many operations involved in the manufacturing of flexible circuitry. Each operation may introduce some error. It is important that these tolerances be

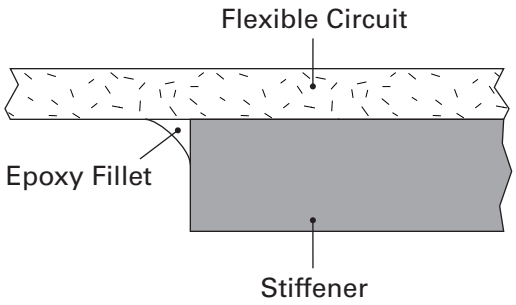


Figure 5-11. Strain relief using an epoxy fillet.

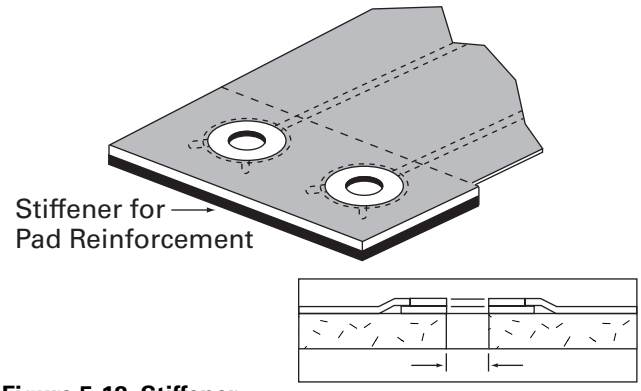


Figure 5-12. Stiffener

considered during the design stage to ensure a circuit design that is both producible and cost-effective.

The flexible laminate used in the processing of flexible circuitry is not highly stable, making it difficult to hold tight tolerances. The growth or shrinkage potential for some of these flexible laminates can be as high as 0.3% depending on environmental conditions. Liberal tolerances should be accommodated whenever possible and where the design allows.

Because of the physical instability of the materials used in the flexible sections relative to the rigid sections, it is important to reference dimensions relative to rigid sections only. As shown in Figure 5-13, the dimension between the two “A” datum is nominally 4.00"; however, since the materials in the flexible section do flex, this dimension cannot be used as a reference with an associated tolerance. Instead, the dimensions should be referenced to some datum located on the rigid section of the assembly, such as the corner or edge, labeled as “AA” in the figure. The length of flex will allow adequate X, Y and Z axis movement for correct positioning of the rigidized areas to the connector or other mounting device. Dimensioning should be limited to standard X and Y linear tolerances in these cases, with the tolerance values appropriate to the design.

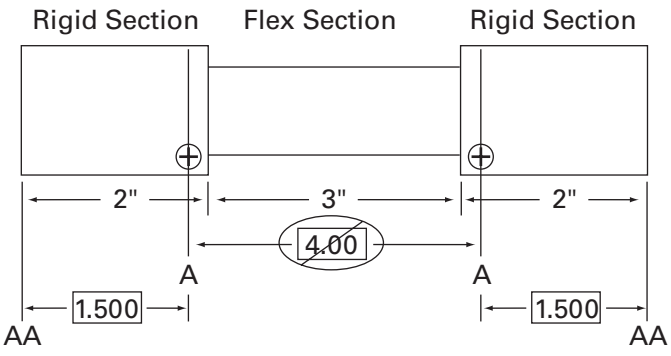


Figure 5-13. Use of datum on rigid section.

Plated-Through Holes

Plated-through holes provide Z-axis interconnects between multiple layers. This is done by terminating innerlayer etch runs with a pad, and then, after final lamination, drilling a through hole in the circuit to allow access to these pads from the outside layers. By plating a coating of conductive material (normally copper) in the through-hole, electrical continuity is provided so that components may be soldered to the surface of the circuit and still interact with conductors that would otherwise be buried. This same method of interconnection is used to link traces from front to back on a double-sided flex circuit; in this case the material is generally predrilled and through-hole plated, and the image is then matched to the drilled holes.

There are some guidelines that should be followed when designing plated-through holes.

1) The plated-through hole diameter should be 0.010" to 0.020" (250µm to 500µm) larger than the diameter of the component lead that is to be inserted and soldered.

a) For components that are to be manually inserted, it is recommended that the holes be 0.010" to 0.012" (250µm to 300µm) larger than the diameter of the component lead.

b) For components that are to be machine inserted, the holes should be 0.015" to 0.020" (375µm to 500µm) larger than the diameter of the component lead to allow for machine positioning tolerances.

These dimensions permit component lead insertion with minimal interference and also provide the proper clearance for sufficient soldering.

2) Plated-through holes should never be used for the mounting of eyelets, stand-off terminals, rivets, or other devices that will place the hole in compression, which will damage the plating in the hole barrel.

3) Care must be taken during innerlayer pad design to provide enough land area on the pad for an annular ring which will provide a good electrical connection to the pad after drilling. Please refer to the *Artwork Design* section of this Guide for additional information on pad termination design.

4) For rigid-flex circuit designs, all plated-through holes should be placed in areas where the hole or the component will not be subjected to any additional stress during bending or flexing. Component holes should not be placed any closer than 0.100" (2.54mm) to the rigid-to-flex interfacial area. This will prevent any components from being placed in close proximity to the flex area. Vias holes can be placed as close as 0.050" (1.25mm) to

the rigid-to-flex interface, but 0.100" (2.54mm) from the interfacial area is preferred.

Non-Plated-Through Holes

Non-plated-through holes, also known as unsupported holes, are used on single- and double-sided circuits for the mounting and soldering of components. The maximum diameter of an unsupported component hole should be not more than 0.020" (500µm) larger than the diameter of the component lead that is to be inserted, unless that lead is to be clinched. The hole diameter should be a minimum of 0.008" to 0.010" (200µm to 250µm) larger than the diameter of the component lead to allow insertion with minimal interference. Proper pad design is important to be sure that there will be sufficient land area to facilitate soldering of the component. Please refer to the section of this Guide titled *Artwork Design* for additional information on pad termination design for unsupported component holes.

Surface Mount Components

Surface mount components should be located on the rigidized sections only on a rigid-flex board. The components edge should not be placed any closer than 0.100" (2.54mm) from the rigid-to-flex interfacial area to prevent any stresses to the component while flexing. Please refer to the applicable IPC manuals for complete specifications governing the design of flexible and rigid-flex circuitry for use with surface mount devices.

Multi-Chip Modules (MCM)

General Design

Fabrication of an MCM-L is very similar to the processes and operations that are used to produce standard printed circuit boards. The design process is also very similar to the steps used when designing a PC board. However, the design rules for feature sizes may change to accommodate the circuit density requirement, so consult with the laminate fabricator regarding their current capabilities prior to designing using these advanced techniques. Electrical and thermal performance must be evaluated so board layout and component placement can be optimized for best results. Environmental conditions, both during assembly and use, must be known so that the designer can choose materials for highest reliability. Prudent use of blind, buried, or micro-vias can increase circuit density without compromising producibility. Narrower line widths should be used where necessary to achieve the circuit routing needed. The addition of circuit layers rather than increasing the routing density on a signal layer may often prove to be the appropriate tradeoff. Assembly issues include not only the next level interconnect, but the board or substrate level as well. Different layout approaches are used for gold wire bonding die directly to a substrate versus flip chip. Once again, consultation with the fabricator will yield better results in the long run.

To ensure that the design supports and accommodates any unique requirements that the assembly and test processes may impose, an understanding of those processes is necessary. Fabricators will often use flying probe testers to test the bare board substrates. Most flying probe testers can test pitch densities as tight as 0.008" (200µm) at the surface. However it may be wise to add test verification points in some locations to assist the test engineer. The board design may also require fiducials to assist in the alignment and set up for wire bonding of bare die to the substrate. If encapsulation is required over the die after bonding, be sure that there is an identified “keep out” area for vias around the device. If underfill will be used, be sure that the component placement will allow for the application and cure of the material.

Surface flatness is much more critical for applications using direct wire-bonds. The layout for copper weights and material thickness must be balanced around the neutral axis or centerline of the board to prevent warp or twist. The same is true for shield and signal layers. Care should be taken to reduce the overall thickness of the laminate substrate to keep the aspect ratio at the plating process as low as possible. Aspect ratio is the comparison of the overall substrate thickness to the diameter of the hole prior to plating. Aspect ratios should not exceed 6:1, otherwise product yield may decrease.

Materials

There are a number of organic materials available for use in printed circuit board fabrication which accommodate a variety of applications and requirements. The material choice will be based largely on the electrical and thermal requirements of the assembly. Epoxy glass, or FR4, is the most commonly used material for fabricating printed circuit boards. This material system exhibits good electrical and physical properties at a relatively low cost. For applications where higher temperature stability is desired, materials such as Bismaleimide triazine (BT resin) or polyimide resin may be used for their high glass transition temperature

DESIRED ELECTRICAL PROPERTIES	
Low dielectric constant	1.0 - 4.0
Homogenous dielectric	Isotropic Properties
Low dissipation factor	≤0.1% for desired frequencies

Table 5-3.

DESIRED PHYSICAL PROPERTIES	
Low moisture absorption	<0.01%
Low rate of moisture absorption	<0.05%
High glass transition temperature (Tg)	> 150 °C
Low CTE (xy-plane)	match Si (3.3 ppm/°C)
Low CTE (z-axis)	match Cu (18ppm/°C)
High Cu adhesion	~ 6lbs/in
High modulus of elasticity	reduce encapsulant induced camber

Table 5-4.

(Tg) properties. Table 5-3 and Table 5-4 show the desirable electrical and physical properties for MCM-L substrate materials.

The use of a low dielectric constant material will enhance signal speed, but less thermally stable materials could lead to reliability concerns by virtue of CTE mismatches of die to the substrate material. It is important to choose materials that will best meet the application with sacrificing critical performance. For example, the CTE delta between silicon and glass-reinforced epoxy material is $11x10^{-5}$. With a temperature delta of 100°C, the result is an 0.011" (275µm) mismatch between the die and the substrate. Table 5-5 provides a comparison of dielectric constant for common substrate materials relative to that of silicon.

Another important, and often overlooked, design requirement is to balance the copper and dielectric thickness around the “neutral axis” or center of the substrate. This is necessary to reduce the tendency of the finished product to warp or deflect during assembly. If soldermask or other type of overcoat is to be applied to the board surface, it should be equally applied to both sides to reduce the tendency of the encapsulant to introduce camber.

MATERIAL PROPERTIES

Material Type	Dielectric Constant	CTE ppm/°C	
		x/y	z
Silicon (SiC)	40	3.7	
Ceramic	7.2	8.1	
Copper	n/a	12	
Epoxy Glass	4.5	15	60
Polyimide	3.6	55	
Teflon Composites			
Ceramic	3.0	17	24
Glass Filled	2.2 - 2.33	31	237
Thermount	3.9	6-9	80/100

Table 5-5.

Thermal Considerations

Heat dissipation is a key player in the reliable operation of an MCM. As temperature increases, either during assembly or operation, materials within a substrate expand at different rates causing thermal stresses both within the substrate itself and at the junction between the substrate and the chips. It is therefore important at the design stage to accommodate the thermal characteristics of the module by allowing for methods of cooling. There are three modes of heat transfer — conduction, convection, and radiation. Radiation cooling is the least efficient; therefore, thermal management efforts at design should focus on convection or conduction cooling.

Poor thermal conductivity through an organic substrate is a major disadvantage for laminate-based MCM’s. As a result, thermal characterization of the laminate substrate is an important part of the design process. Modeling of multilayered printed circuit boards is both more critical and more complex considering the varied materials found in a typical PCB. Software packages are available to perform thermal analysis based on the thermal conductivity of the materials used but they require analyzing each material independently, a task that is arduous and produces questionable results. One method often practiced to model this complex heat transfer problem is to lump the conductive properties of the individual layers into a single, effective thermal conductivity, K_{eff}. Designers can then perform the thermal

characterization of the composite using this single value to simplify the process. Table 5-6 lists the thermal dissipation values for various materials used in MCM's.

Power device placement is a prime example of a potential heat source on a substrate. During operation these devices generate a higher heat profile than other components. Power devices, or other potential heat sources should be separated from each other to minimize localized temperature rises. To help identify areas of concern computer thermal modeling can be used that would identify areas that may generate excessive heat. Thermal vias are used to channel heat through the board to reduce localized hot spots. The vias can either connect to an external heatsink or to large innerlayer planes of copper that act as heat spreaders for better transfer of heat through conductive cooling.

THERMAL CONDUCTIVITY OF VARIOUS MATERIALS

Material Type	k (W/mK)
Silicon (SiC)	270
Ceramic (Al2O3)	30
Copper	386.0
Epoxy Glass (FR4)	0.41
Polyimide Film	2.87×10^{-4}*
Teflon Composites	
Ceramic Filler	0.50
Glass Filler	0.20
Thermount (epoxy)	0.187

*Polyimide film value expressed cal/cm sec K units

Table 5-6.

Simplified Thermal Analysis

As an example of this simplified method, an analysis can be performed for one dimensional heat flow from a steady source of heat through a material with a constant thermal conductivity. Figure 5-14 shows the cross-section of the multiple layers that make up the MCM used in this example. Under these conditions, Fick's first law states that the thermal conductivity is given by:

$\Delta Q/\Delta t = kA\ \Delta T/\Delta x$

In other words, the heat flow is proportional to the temperature gradient, DT/Dx, and the area of the heat flow, A. The proportionality constant is the thermal conductivity of the material, k. For a chip mounted on a thin sheet of material, Dx is just the sheet thickness d, and the heat generated is equal to the power dissipated, P. The temperature difference DT across the sheet is simply:

$\Delta T = Pd/(kA)$

No information relative to the time it takes to develop this temperature differential is included in the above, but for electronic systems design, only the perceived maximum temperatures are of concern. As long as the conductance has a single main direction, contributions of different layers may be added.

As a first assessment on the temperature difference to develop across the substrate stack shown in Figure 5-14, vias and lateral heat dissipation may be neglected, and the area may be assumed to have the same size as that of the chip. The largest DT will arise from the chip with the highest power density, P/A.

Assume the system we are analyzing has three chips with power densities as shown in Table 5-7.

POWER DENSITIES

Chip	Power (W)	Chip Size (mil)	Area (cm^2)	P/A (W/cm^2)
#1	0.65	211	0.287	2.26
#2	2.40	238	0.397	6.05
#3	0.75	140	0.127	5.93

Table 5-7.

The highest value is exhibited by Chip #2; the smaller Chip #3 has almost the same power density.

The thermal conductances of the polymeric materials, namely the polyimide and prepreg layers, are no larger than 0.19 W/mK. That results in a temperature differential of about 15°C per prepreg/polyimide layer, or a total temperature difference of 180°C across the eight (8) prepreg and four polyimide layers. See Figure 5-14. Despite the alleviating factor that electrical copper vias are going to reduce this difference, it cannot be assumed that the maximum permissible temperature difference of 50°C might be maintained with this design.

As a result of this estimate, thermal vias will be introduced into the design, as shown in Figure 5-15. In this example, the thermal vias are designed to have an outer diameter of 0.008" (200µm), and a plating thickness of 0.001" (25µm). The copper cross section of these vias is 0.0134 mm^2 per via. A total of 16 vias are

Material	Thickness (mil)
Solder mask	1.0
Copper	1.2
Polyimide	2.0
Copper	1.2
Prepreg	1.8
Prepreg	1.8
Copper	1.2
Polyimide	2.0
Copper	1.2
Prepreg	1.8
Prepreg	1.8
Prepreg	1.8
Copper	1.2
Polyimide	2.0
Copper	1.2
Prepreg	1.8
Prepreg	1.8
Copper	1.2
Polyimide	2.0
Copper	1.2
Prepreg	1.8
Total:	36±4

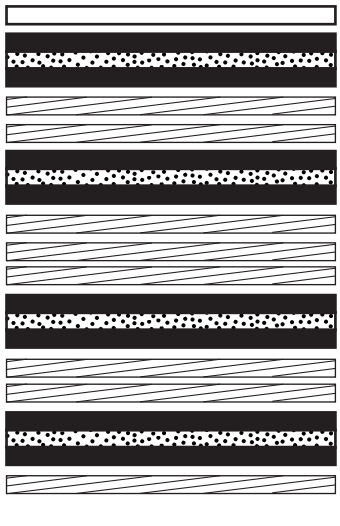


Figure 5-14. Original Layer Stack-up.

introduced under Chip #1, 89 under Chip #2, and 41 under Chip #3. These vias are intended to end above the last layer of the prepreg, to assure good isolation between the different backside potentials of the chips involved. In this configuration, more than 75% of the temperature differential occurred in this last prepreg layer.

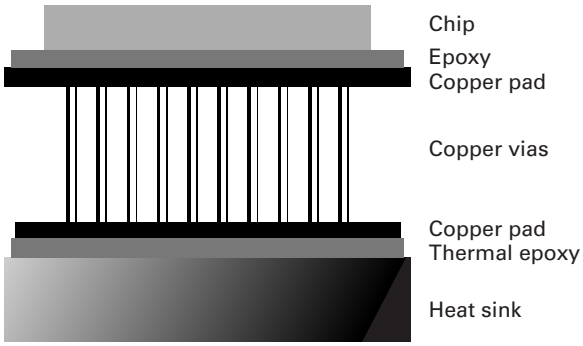


Figure 5-15. Configuration used for thermal modeling.

In this example which is taken from an actual manufactured product, the customer chose to minimize thermal resistance by mounting the entire substrate with a 0.002" (50µm) thick layer of thermally conductive epoxy adhesive onto their heat sink. Refer to Figure 5-15. To have good thermal contact from the end of the vias, a lateral heat-spreading copper pad was necessary. At a thickness of 0.0012" (30µm), it may be approximated as a thermal conductor with its full area. Here, a slightly higher temperature gradient for the spreading is realistic, but as the entire temperature difference built up in this layer is extremely small, this complication can be disregarded.

The following tables give the results of this model for the three chips in this example. For Chip #1, a total temperature difference of only 6.3°C is predicted, roughly half of it due to the thermal vias, the other half due to the epoxy layers. As the number of thermal vias has not increased proportionally to the power of Chip #2, the temperature drop across the vias is higher, leading to an overall DT of slightly below 8°C. For Chip #3, the very small number of thermal vias creates a relatively high temperature gradient, so that the overall heating effect is about the same for all three chips. The heating of less than 10°C is an excellent example for the possibilities of laminate technologies, if appropriate use is made of the technological options.

Board Layout

During the layout phase of the board design, power and ground layers are distributed throughout the laminate structure as planes and connected to each other and the critical signal paths through plated vias. These vias are either drilled through holes, blind vias to connect a surface layer to an internal layer, or buried vias that connect internal layers to each other, although the latter will increase processing difficulty. Circuit routing density is primarily dependent on the pad pitch that can be achieved, specifically in the areas where the die will be placed. Advances in high density circuit routing have been made possible by incorporating the use of microvias allow for pad densities as high as 350 pads/inch. The use of finer pitch components requires a reduction in the trace width and spacing width as well. Traditional circuit board densities for surface mount devices require trace width and spacing on the order of 0.007" (175µm). For chip-on-board MCM-L applications, where routing may be required to four rows of pads for high I/O devices, 0.002" (50µm) trace width and spacing may be required.

It is important to balance the essential features of the design with the fabricators' capabilities and not design a product that is extremely difficult to manufacture. Features such as via diameter, trace and space width, registration tolerance/pad size, and number of layers are all interrelated; changes to one of these features imply changes to one or more of the others to maintain the same routing density.

Component or Die Placement

Components need to be carefully placed on the substrate with consideration given to electrical performance and thermal requirements. Sensitive components should be

CHIP 1

Layer	d (mm)	P (W)	k (W/mK)	A (mm2)	DT (°C)
Conductive Epoxy	0.025	0.75	1.2	12.7	1.230
Copper	0.0305	0.75	390	12.7	0.0046
Copper vias	0.84	0.75	390	0.5635	2.867
Copper pad	0.0305	0.75	390	12.7	0.0046
Thermal Epoxy	0.045	0.75	1.2	12.7	2.215
				Total:	6.321

CHIP 2

Layer	d (mm)	P (W)	k(W/mK)	A (mm2)	DT (°C)
Conductive Epoxy	0.025	2.40	1.2	39.7	1.260
Copper	0.0305	2.40	390	39.7	0.0047
Copper vias	0.84	2.40	390	1.2232	4.226
Copper pad	0.0305	2.40	390	39.7	0.0047
Thermal Epoxy	0.045	2.40	1.2	39.7	2.267
				Total:	7.762

CHIP 3

Layer	d (mm)	P (W)	k(W/mK)	A (mm2)	DT (°C)
Conductive Epoxy	0.025	0.65	1.2	28.7	0.472
Copper	0.0305	0.65	390	28.7	0.0018
Copper vias	0.84	0.65	390	0.22	6.364
Copper pad	0.0305	0.65	390	28.7	0.0018
Thermal. Epoxy	0.045	0.65	1.2	28.7	0.849
				Total:	7.688

Table 5-8.

isolated from components that may cause interference. Bare die must be spaced appropriately to allow for encapsulation after assembly. Land pattern geometries and pitch densities have to allow adequate space for die and component placement. Typical pitch spacing for chip-on-board devices on laminate are:

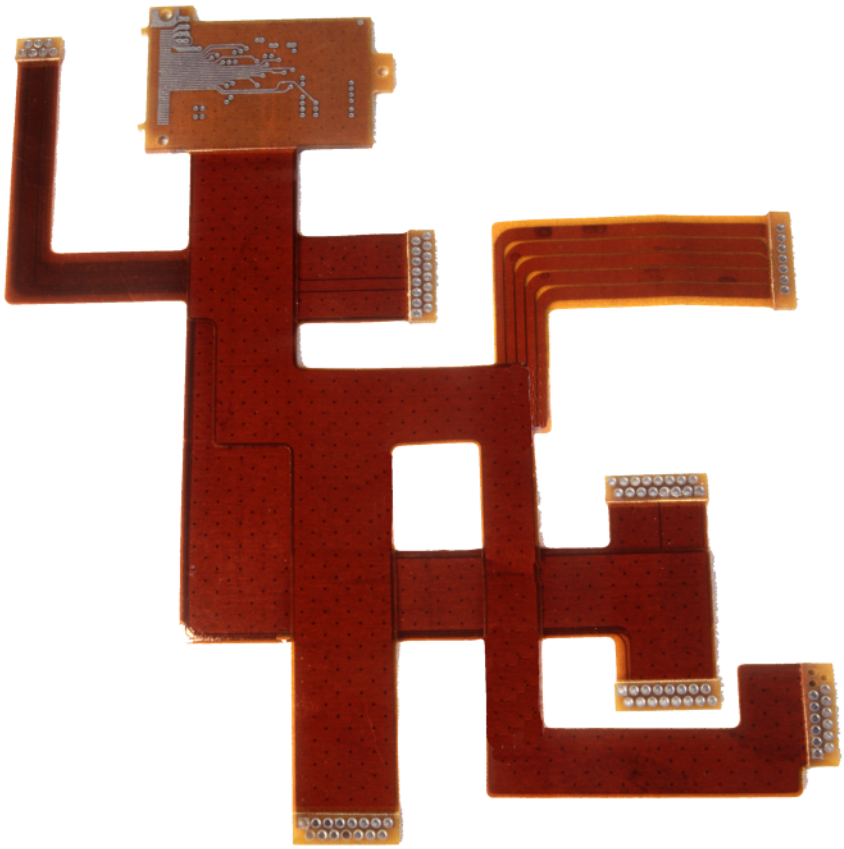
- Pitch spacing = 0.012" (300µm) on center
- Land widths = 0.006" - 0.008" (150µm - 200µm)
- Land spacing = 0.004" - 0.006" (100µm - 150µm)

The bond pad must also be large enough to permit one or more rework operations since it may be impossible to achieve a good bond in the exact same site from which a wire was removed. If components such as SMT or BGA packages are used, provisions for rework must be incorporated.

Wire Bonding to MCM-L Substrates

Both aluminum and gold wire bonds have been used to successfully connect die to an MCM-L substrate. Aluminum wedge bonding requires a temperature less than 100°C and has been successfully used for consumer applications. Gold wire bonding is currently the most prevalent attachment method and requires a temperature of 150°C which is higher than the Tg of some FR4 materials (~125°C). For applications in which there are a high number of bond pads, this could lead to a reliability concern as the FR4 material is held at a temperature above its Tg for an extended period of time. For these applications, it would be wise to choose a surface material with a higher Tg such as Polyimide or BT resin. For both types of wire bonding, the surface finish is usually 0.50µm to 1.0µm barrier layer of low stress nickel plating over the copper traces. The final plating is typically specified as 99.9% purity, soft electrolytic gold plate, 0.5µm to 0.75µm thick.

Module rework is a major concern when using direct die attachment to laminate substrates. The use of an adhesive that is reworkable is strongly recommended. During rework the gold wires are either pulled or cut to facilitate the removal of the defective die. Heat is then applied to soften the adhesive and the component is removed. Special care must be taken to not degrade the bond pad adhesion during the rework procedure. This is accomplished by limiting the time the unit is above the materials Tg during rework or repair.



Product Example

6

Artwork Design

Chapter Terms

Annular Ring: That portion of a conductive material completely surrounding a hole.

Cover Lay or Covercoat: The layer of insulating material that is applied over a conductive pattern on the outer surface of a printed circuit. Used for electrical insulation and environmental sealing.

Dielectric: A material with a high resistance to the flow of electrical current.

Delamination: A separation between plies within a base material, between a base material and a conductive foil, or any other planar separation within a multi-layer printed board.

Gerber Data: A type of data that consists of aperture selection and operation commands and dimensions in X- and Y-coordinates. The data is generally used to direct a photopolotter in generating photoplotted artwork.

Hold Down Tabs: Conductive tabs extending from the outside of an annular ring or other termination pad used to help secure the pad to the substrate.

Plated-Through Hole: A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board.

Terminal Pad: A portion of a conductive pattern that is usually used for making electrical connections, for component attachment, or both.

Unsupported Hole: A hole that does not required plating-through. Most often found in single- and double-sided circuits.

Regardless of the care taken in the overall design, whether a finished flexible circuit meets the overall requirements of the system or not is ultimately determined by the artwork used to produce the etched pattern. In the artwork, all the conductor runs are laid out, the termination areas defined, and the periphery dimensions outlined. It is important to have all the electrical and mechanical parameters well defined prior to starting the artwork design. Please refer to the *Electrical Design* and *Mechanical Design* sections of this Design Guide before starting the actual artwork design.

Automated Artwork

CAD/CAM design workstations find increasing use in flexible circuitry design and manufacturing. CAD/CAM equipment can produce the artwork master patterns, mechanical drawings, and drill programs. CAD/CAM workstations also result in the best layer-to-layer registration for multi-layer and rigid-flex designs. The computer allows the designer to design various layers to a master pad pattern for maximum registration accuracy. To reduce lead times and provide more dimensionally accurate tooling, Teledyne Electronic Technologies has set up data-link workstations to send computer files directly to tooling vendors via the internet.

Supplied Artwork

For designs that are already complete, the CAD/CAM computer can still be used to make any necessary changes to assure manufacturability of the circuitry. This is accomplished by either reading the data directly electronically, or by scanning an existing artwork master and translating the information to an electronic file for input into the designer's data base. The second method is not preferred and should be used only as a last resort due to overall accuracy issues. The supplied data is verified for produceability, and modified if needed.

General Artwork Design Rules

Conductor Widths

Flexible circuit designers use nomographs to determine:

- conductor widths
- conductor thicknesses
- equivalence to round wire gages
- width and thickness necessary for a maximum 10°C temperature rise due to the current carried
- cross-section required for a specific voltage drop

The appropriate graphs and nomographs to assist in determining these parameters can be found in the *Electrical Design* section of this Guide.

In general, all flat rolled annealed copper foil will have some etch loss during processing. Teledyne Electronic Technologies adds an etch loss factor to conductors in the artwork. Table 6-1 lists typical etch loss compensation for various copper thicknesses. The figures presented are considered conservative; current manufacturing processes yield somewhat better results.

ETCH LOSS FACTORS

Ounce Weight Copper	Compensation (Minimum)	(Minimum)
1/2	+ 0.0005"	12.5µm
1	+ 0.001"	25µm
2	+ 0.002"	50µm
3	+ 0.003"	75µm
4	+ 0.004"	100µm

Table 6-1.

Using the factors in this table, a minimum conductor width of 0.011" (275µm) would be used to obtain a 0.010" (250µm) finished conductor width using one ounce copper. Good design practice maximizes the copper on the circuit where possible, without affecting electrical characteristics.

Conductor Spacing

Spacing requirements for a flexible circuit are determined by the desired electrical characteristics of the design. Please refer to the *Electrical Design* section of the Guide for additional information on spacing requirements. The artwork should be designed, as a minimum, with the actual spacing required.

Because etching on flexible circuitry is a subtractive process, it is good practice to allow as much space as possible and still meet the electrical and mechanical constraints of the system to account for irregularities in the etching process.

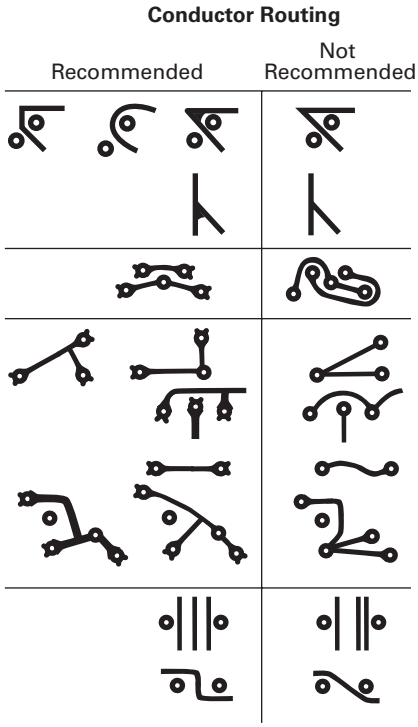


Figure 6-1. Conductor routing examples.

Conductor Routing

There are several design practices that should be employed during the conductor routing phase to be sure that the artwork is designed for maximum manufacturability and also meets the mechanical constraints of the application:

1) as mentioned in the *Mechanical Design* section of this Design Guide, all conductors should run perpendicular to the fold line for any circuit that will be bent or formed in use.

2) when establishing conductor routing, the designer must avoid using acute internal angles, which can trap etching acid causing improper etching. Also, sharp external angles should be avoided as they tend to cause delamination by concentrating forces at one point.

3) when conductors enter into a pad area, it is important to maintain equal spacing where the conductors pass between the lands. It may be necessary to change either the pad configuration or the conductor width or configuration. Examples of optional configurations are shown in Figure 6-3.

4) artwork should be designed with a balanced circuitry pattern where possible. Large open areas or congested conductor runs should be redesigned for even conductor placement. The circuit design in Figure 6-2 shows both an improper design and a proper design with even conductor placement.

For double-sided circuits or multi-layer combinations that use double-sided innerlayers, the conductors and spacing should alternate on opposite sides as shown in Figure 6-4. This allows maximum flexibility without putting additional stress on the copper conductors.

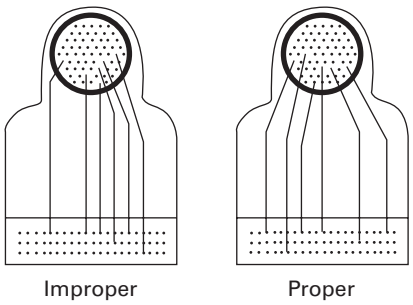


Figure 6-2. Balanced circuitry will improve producibility and flexibility.

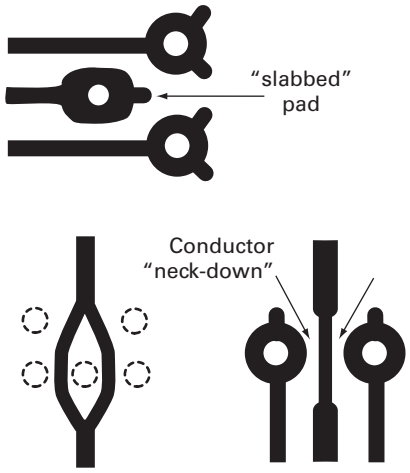


Figure 6-3. Various configurations may be used to maintain equal conductor spacing.

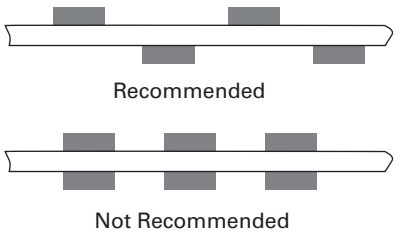


Figure 6-4. Offsetting conductors on opposite sides of the circuit will reduce stresses in flexing applications.

Terminal Construction

Termination pads or fingers should be as large as possible without violating spacing requirements. Terminal areas must be designed to accommodate the fabrication allowances inherent in the current manufacturing capabilities of the fabricator. As shown in Figure 6-5, the final size of the terminal area is determined by the relationship among several factors:

- the size of the terminal hole
- the allowance for drilling tolerance
- twice the minimum dimension for the annular ring surrounding the hole
- the fabrication allowance for standard (versus reduced) producability

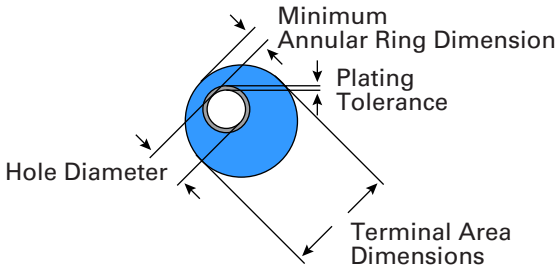


Figure 6-5. FAB Allowance.

In the example in Figure 6-5, the size of the terminal area is determined by Table 6-2.

PAD SIZE CALCULATION

Criteria	Dimensions	
finished hole size	0.020"	500µm
plating tolerance	+0.005"	+125µm
2x minimum annular ring dimension	+0.004"	+100µm
standard fabrication allowance	+0.015"	+375µm
termination area diameter	= 0.044"	= 1.10mm

Table 6-2.

All pads should incorporate the use of a fillet where the conductor enters the pad as shown in Figure 6-6. This fillet will provide adequate strain relief between a conductor and the pad area without impacting conductor width or spacing requirements.

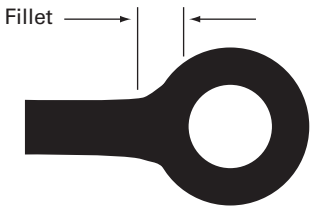


Figure 6-6. Pad-to-conductor strain relief fillets.

Annular Ring

When designing pad terminations, it is important to account for both the annular ring requirements of the circuit and the hole-to-pad ratio. The annular ring is the circular strip of conductive material that surrounds a hole.

For unsupported, or non-plated-through holes, the desired annular requirement is 0.015" (375µm) minimum. The annular ring can be less than this only if the pad is anchored by hold down tabs or if the land is elongated to provide an equivalent soldering surface. Please refer to the following section titled *Termination Pad Design for Non-Plated-Through Holes.*, for additional information.

For supported, or plated-through holes, annular ring considerations fall into two classifications.

- The external annular ring, as the name suggests, is on outside layers and in areas that will be solder coated. The annular ring on external layers is the minimum amount of copper, at the narrowest point, between the edge of the hole and the edge of the land. The minimum external annular ring should measure 0.005" (125µm) for double-sided circuits requiring plating and for multi-layer and multi-layer rigid-flex circuits. This will allow for soldering any components to the surface.
- The internal annular ring is the amount of the pad that remains after the hole has been drilled. The amount of internal ring remaining is important to the electrical and mechanical integrity of the plated-through hole. Internal annular rings for multi-layer flex and rigid-flex should be 0.002" (50µm) minimum. In applications where tight hole-to-pad ratios exist, it is permissible to have

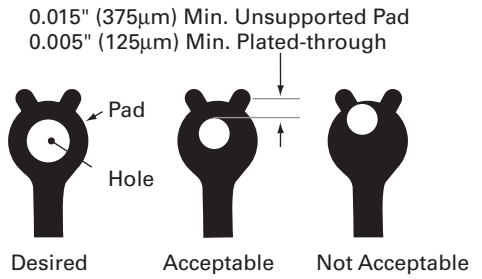


Figure 6-7. Annular rings minimum dimensions.

less than a 0.002" (50µm) internal annular ring, as long as the hole connection is not compromised.

Termination Pad Design for Non-Plated-Through Holes.

Holes that do not require plating-through are termed unsupported holes. They are most commonly found in single- and double-sided circuits. Pad design for unsupported holes must account for encapsulation of the pad by the covercoat to prevent pads from lifting. This can be accomplished in several ways:

- by incorporating fillets and hold-down ears, as shown in Figure 6-8, the covercoat openings can be as large as the land area, permitting the maximum amount of pad exposure. A pad that does not incorporate hold down tabs and fillets should have a covercoat overlap onto the pad of 0.010" (250µm) minimum. This will reduce the amount of solderable annular ring or require the use of larger diameter pads.

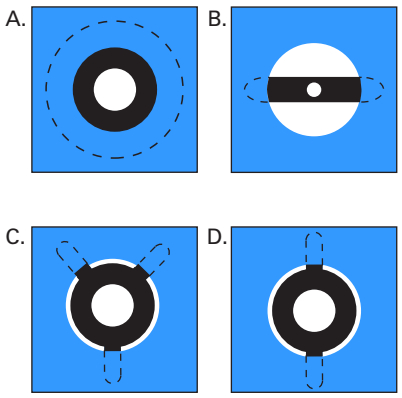


Figure 6-8. Pad tie-down methods.

A. Pad overlapped by covercoat insulation 0.020" (500µm) for 360°.

B. Elongated pad allows tighter pad densities with sufficient pad encapsulation.

C. & D. Fillets and hold-down ears permit the covercoat opening to be as large as the pad for maximum pad exposure.

- by using a finger or rectangular pad configuration. The view in Figure 6-9 shows this type of terminal area which is used when access to the flexible circuitry is desired in the vertical plane. This style of termination would be used when lap soldering pins flat to a circuit.

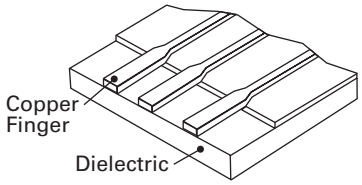


Figure 6-9. Vertical access using rectangular pads.

Nomenclature Artwork and Component Designation

To assist in component placement during assembly and identification during service, it may be necessary to incorporate component designation in the artwork during the design stage. The most cost-effective method of component identification is to incorporate the designations as part of the etched artwork. Care should be taken regarding placement of the designations so as not to compromise electrical testing. For single-sided or double-sided applications, the etched nomenclature can be placed in any appropriate area. For multi-layer flex and rigid-flex the etched nomenclature is best placed in the bonded or rigidized areas on the outer layer artwork. The lettering should be designed as large as possible to assure clarity after etch. Care should be taken not to violate any spacing requirements.

Due to the high circuit density, nomenclature in surface mount applications is typically applied with silk screen artwork and epoxy ink. The screened nomenclature on the artwork should be designed as large as possible for clarity. Care should be taken to not place nomenclature over any areas that will be solder coated to prevent distortion during the assembly process. Component orientation must be considered to assure that no nomenclature will be covered by any part of the components or hardware. Understanding of the formed configuration is also important so that all pertinent marking will be visible after forming and final installation. Finally, placement of nomenclature should include information to aid in electrical testing.

7

Design Checklists

Electrical Design Checklist

Use the following checklist to confirm that your circuit design will provide maximum interconnect performance and producibility. And be sure to enlist the consultation of our design and manufacturing engineers before finalizing your specifications. Our extensive experience with electronic interconnection designs can provide the most cost-effective solution for your packaging needs.

The design should specify the conductor width, conductor spacing and conductor thickness.

- ❑ Is the minimum width sufficient for current requirements?
- ❑ Is the minimum width sufficient for resistance requirements?
- ❑ Is the minimum spacing sufficient for voltage requirements between conductors?

For designs requiring transmission line properties, such as impedance and capacitance control, the design will need to specify the values required for:

- ❑ dielectric requirement between layers.
- ❑ dielectric requirement between conductors.

Mechanical Design Checklist

Use the following checklist to confirm that your circuit design will provide maximum interconnect performance and producibility. And be sure to enlist the consultation of our design and manufacturing engineers before finalizing your specifications. Our extensive experience with electronic interconnection designs can provide the most cost-effective solution for your packaging needs.

Fold Areas

- ❑ Do conductors run perpendicular to the fold?
- ❑ Has extra copper been added to help hold the formed shape when folded?
- ❑ For multi-layer and rigid-flex circuits, is the bend radius a minimum of 12 times greater than the circuit thickness?
- ❑ Are tear stops utilized where folds end internally?

Circuit Profile

- ❑ Is sufficient edge distance specified to cover the minimum spacing requirement plus additional profiling tolerances?
- ❑ Are all internal corners radiused and reinforced with tear stops?
- ❑ Are all external corners chamfered or radiused?

Stiffeners and Reinforcements

- ❑ Are stiffening location marks utilized on the artwork?
- ❑ Are hole diameters in the stiffeners a minimum of 0.014" (350µm) larger than the through hole in the circuit?
- ❑ Has strain relief been specified to form a radius at the edge of thick stiffeners?
- ❑ Has the adhesive for bonding the stiffener been specified?
- ❑ Have mounting holes been provided?
- ❑ Have potential rub or wear areas been reinforced?

Tolerances

- ❑ Are all tolerances specified on the master drawing?
- ❑ Are tolerance ranges liberal enough to allow for cost-effective manufacturing?
- ❑ Are tolerances generated from a zero reference point to prevent a stack-up of tolerances?

Mechanical (con't)

Environmental

- ❑ Have operating and maximum temperatures been defined?
- ❑ Have materials been chosen that will support the application for:
  - reflow?
  - wave solder assembly?
  - moisture absorption?
  - tensile strength?
  - flammability?
  - thermal cycling?

Artwork Design Checklist

Use the following checklist to confirm that your circuit design will provide maximum interconnect performance and producibility. And be sure to enlist the consultation of our design and manufacturing engineers before finalizing your specifications. Our extensive experience with electronic interconnection designs can provide the most cost-effective solution for your packaging needs.

Conductors

- ❑ Are the conductors parallel and consistent in width?
- ❑ Are the conductors on double-sided circuits and double-sided innerlayers offset from top to bottom?
- ❑ Are conductors centered between holes and pads?
- ❑ Have conductors been routed in the shortest possible paths?
- ❑ Have conductors been designed to avoid acute internal and external angles?
- ❑ Have the conductors been routed in such a way as to avoid passing between two used pads in connector areas?

Shielding

- ❑ Have guard conductors been used to isolate certain conductors?
- ❑ If full shielding is specified, have cross-hatched patterns in flex areas been utilized?

Terminal Pads

- ❑ Do all pads have fillets?
- ❑ Do pads for unsupported holes have tie-down ears?
- ❑ Are pads large enough to account for annular ring requirements?
- ❑ 0.015" (375µm) for unsupported holes.
- ❑ 0.005" (125µm) for double-sided supported holes.
- ❑ 0 005" (125µm) for external annular ring on multilayer flex.
- ❑ 0.002" (50µm) for internal annular ring on multilayer flex.

8

Glossary

A

Acceptance Tests: Those tests deemed necessary to determine the acceptability of a product and as agreed to by both purchaser and vendor.

Access Hole: A hole or series of holes in successive layers of a multilayer board. These holes provide access to the surface of the land on one of the layers of the board.

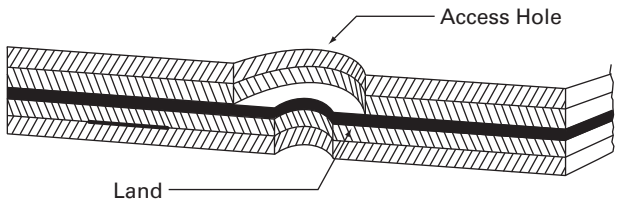


Figure 8-1. Access Hole

Adhesiveless Laminates: A copper-clad composite of polyimide film bonded to copper foil.

Alignment Mark: A stylized pattern that is selectively positioned on a base material to assist in alignment.

Anchoring Spur: An extension of a land on a flexible printed board that extends beneath the cover lay to assist in holding the land to the base material.

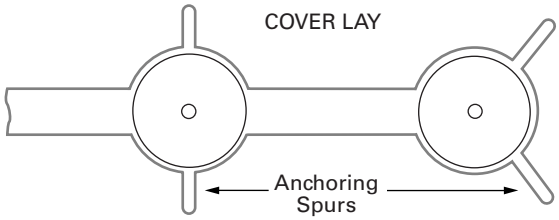


Figure 8-2. Anchoring Spur

Annular Ring: That portion of conductive material completely surrounding a hole.

Artwork: An accurately-scaled configuration that is used to product the "Artwork Master" or "Production Master".

Artwork Master: An accurately-scaled, usually 1:1, pattern that is used to produce the "Production Master".

Aspect Ratio (Film): The ratio of the length of a film component to its width.

Aspect Ratio (Hole): The ratio of the length or depth of a hole to its pre-plated diameter.

Assembly: A number of parts, subassemblies, or combinations thereof joined together. (Note: This term can be used in conjunction with other terms listed herein, e.g., "Printed Board Assembly".)

Assembly Drawing: A document that depicts the physical relationship of two or more parts, a combination of parts and subordinate assemblies, or a group of assemblies required to form an assembly of a higher order.

Asymmetric Stripline: A stripline signal conductor that is embedded, but not centered, between two ground planes.

Automatic Test Equipment: Equipment that automatically analyzes functional or static parameters in order to evaluate performance.

AWG Equivalent: The American Wire Gauge (AWG) round-conductor number that is used to designate a flat conductor with an equal cross-sectional area.

B

Back-Bared Land: A land in flexible printed wiring that has a portion of the side normally bonded to the base dielectric material exposed by a clearance hole.

Backplane: An interconnection device used to provide point-to-point electrical interconnections. (It is usually a printed board that has discrete wiring terminals on one side and connector receptacles on the other side.) (See also, "Mother Board")

Bake Out: Subjecting a product to an elevated temperature in order to remove moisture and unwanted gasses prior to final sealing.

Barrel Cracks: Cracks that appear in the electro-plating inside a plated through hole due to mechanical and thermal stresses.

Base Material: The insulating material upon which a conductive pattern may be formed.

Base Material Thickness: The thickness of the base material excluding metal foil or other material deposited on its surfaces.

Basestock: See "Base Material"

Blind Via: A via extending from an inner layer to an outer layer of a printed circuit board.

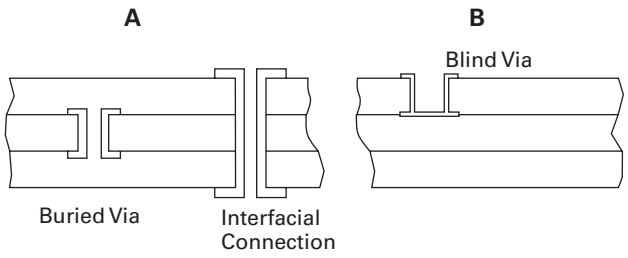


Figure 8-3. Vias (buried, through-hole and blind)

Blister: Delamination in the form of a localized swelling and separation between any of the layers of a laminate base material, or between base material and conductive foil or protective coating.

Board Thickness: The overall thickness of the base material and all conductive materials deposited thereon.

Bond Enhancement Treatment: The improvement of the adhesion of a metal foil surface to an adjacent layer of material to which it is being attached.

Bow (Printed Board): The deviation from flatness of a board characterized by a roughly cylindrical or spherical curvature such that, if the board is rectangular, its four corners are in the same plane. (See Figure 8-4.)

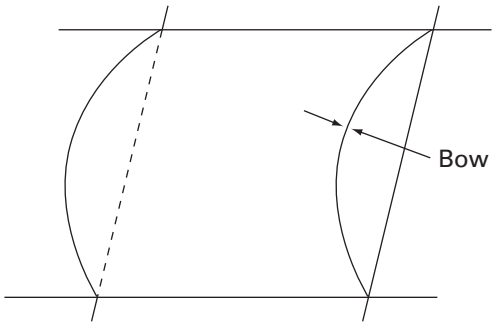


Figure 8-4. Bow

B-Stage: An intermediate stage in the reaction of a thermosetting resin in which the material softens when heated and swells, but does not entirely fuse or dissolve, when it is in contact with certain liquids. (Also see "C-Staged Resin".)

Buried Via: A via that does not extend to either surface of a printed board. (See Figure 8-3.)

C

C-Staged Resin: A resin in its final state of cure.

Cap Lamination: The bonding process of making a multilayer printed board with surface layers of single-sided metal-clad base material laminated with other base materials in a single operation. (See also, "Foil Lamination".)

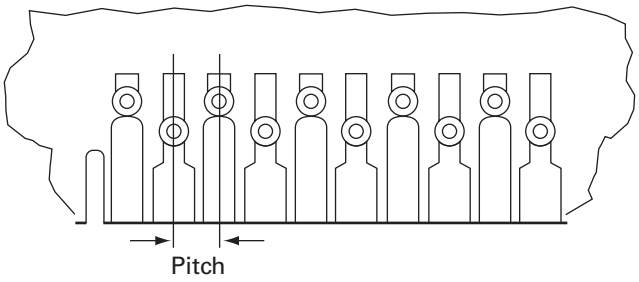


Figure 8-5. Center-to-Center Spacing

Center-to-Center Spacing: The nominal distance between the centers of adjacent features on any single layer of a printed board. (See Figure 8-5.) (See also "Pitch".)

Characteristic Impedance: The ratio of voltage to current in a propagation wave, i.e., the impedance which is offered to a propagation wave at any point of the line.

Check Plot: An interim drawing used for graphical data verification.

Circuit: A number of electrical elements and devices that have been interconnected to perform a desired electrical function.

Circuitry Layer: A layer of a printed board containing conductors, including ground and voltage planes.

Clad (adj.): A condition of the base material to which a relatively-thin layer or sheet of metal foil has been bonded to one or both of its sides, e.g., "a metal-clad base material".

Clearance Hole: A hole in a conductive pattern that is larger than, and coaxial with, a hole in the base material of a printed board.

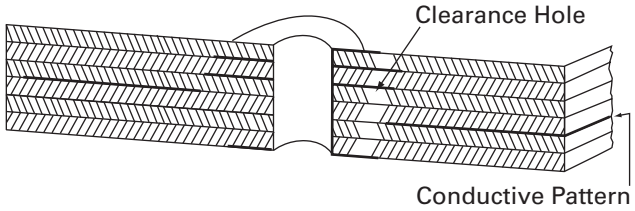


Figure 8-6. Clearance Hole

Coaxial Cable: A cable in the form of a central wire surrounded by a conductor tubing or sheathing that serves as a shield and return.

Coefficient of Thermal Expansion (CTE): The linear dimensional change of a material per unit change in temperature. (See also "Thermal Expansion Mismatch".)

Cold Solder Connection: A solder connection that exhibits poor wetting and that is characterized by a greyish porous appearance. (This is due to excessive impurities in the solder, inadequate cleaning prior to soldering, and/or the insufficient application of heat during the soldering process.)

Compensated Artwork: Production master or artwork data that has been enlarged or reduced in order to meet the needs of subsequent processing requirements.

Component Density: The quantity of components on a unit area of printed board.

Component Hole: A hole that is used for the attachment and electrical connection of component terminations, including pins and wires, to a printed board.

Component Lead: The solid or stranded wire or formed conductor that extends from a component to serve as a mechanical or electrical connector, or both. (See also "Component Pin".)

Component Mounting: The act of attaching components to a printed board, the manner in which they are attached, or both.

Component Mounting Orientation: The direction in which the components on a printed board or other assembly are lined up electrically with respect to the polarity of polarized components, with respect to one another, and/or with respect to the board outline.

Component Pin: A component lead that is not readily formable without being damaged. (See also "Component Lead".)

Component Side: The primary side of a single-sided assembly.

Composite (Phototool): A photograph that consists of combination two separate (aligned) images.

Computer-Aided Design (CAD): The interactive use of computer systems, programs, and procedures in the design process wherein, the decision-making activity rests with the human operator and a computer provides the data manipulation functions.

Computer-Aided Engineering (CAE): The interactive use of computer systems, programs, and procedures in an engineering process wherein, the decision-making activity rests with the human operator and a computer provides the data manipulation functions.

Computer Numerical Control (CNC): A system that utilizes a computer and software as the primary numerical control technique.

Conductive Foil: A thin sheet of metal that is intended for forming a conductive pattern on a base material.

Conductive Pattern: The configuration or design of the conductive material on a base material. (This includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the printed board manufacturing process.)

Conductivity: The ability of a substance or material to conduct electricity.

Conductor: A single conductive path in a conductive pattern.

Conductor Base Width: The width of a conductor at the plane of the surface of a base material. (See also "Conductor Width" and "Design Width of Conductors".)

Conductor Layer No.1: The first layer of a printed board that has a conductive pattern on or adjacent to its primary side.

Conductor Layer: The total conductive pattern formed on one side of a single layer of a base material. (This may include all or a portion of ground and voltage planes.)

Conductor Side: The side of a single-sided printed board that contains the conductive pattern.

Conductor Spacing: The observable distance between adjacent edges (not center-to-center spacing) of isolated conductive patterns in a conductor layer. (See also "Center-to-Center Spacing".)

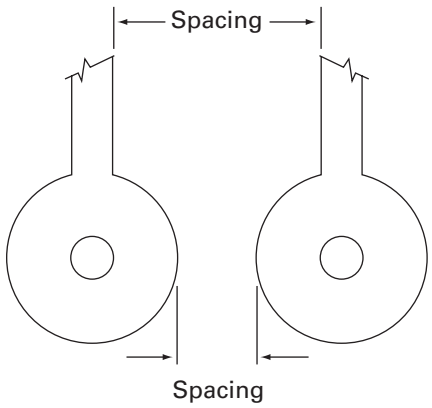


Figure 8-7. Conductor Spacing

Conductor Thickness: The thickness of a conductor including all metallic coatings and excluding all protective coatings.

Conductor Width: The observable width of a conductor at any point chosen at random on a printed board as viewed from directly above unless otherwise specified. (See also "Design Width of Conductors" and "Conductor Base Width".)

Conformal Coating: An insulating protective covering that conforms to the configuration of the objects coated when it is applied to a completed printed board assembly.

Connector: A device used to provide mechanical connect/disconnect service for electrical terminations.

Connector Area: That portion of printed wiring used for the purpose of providing external connections.

Connector Contact: The conducting member of a connecting device that provides a separable connection.

Connector Housing: A plastic shell that holds electrical contacts in a specific field pattern that may also have polarization/keying bosses or slots.

Continuity: An uninterrupted path for the flow of electrical current in a circuit.

Copper Clad Laminate: Metal-clad base material that has copper as the conductive material.

Corner Marks: The marks at the corners of artwork whose inside edges establish, or help to establish, the borders and contour of a printed board.

Coupon (Breakaway): Coupons made as an integral part of the end product board and connected as one piece, except one edge of the coupon has perforations or a thin section connected to the board which can be easily broken off without damaging either the coupon or the board.

Cover Lay: The layer of insulating material that is applied over a conductive pattern on the outer surface of a printed board.

Crazing: An internal condition that occurs in reinforced laminate base material whereby glass fibers are separated from the resin at the weave intersections. (This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to mechanically-induced stress.) (See also “Measling”.)

Crease: A ridge in a material that is caused by a fold or wrinkle being placed under pressure.

Crimp Contact: A type of connector contact whose non-mating end is a hollow cylinder that can be crimped onto a wire inserted within it.

Crosshatching: The breaking up of large conductive areas by the use of a pattern of voids in the conductive material.

Crosstalk: The undesirable interference cause by the coupling of energy between signal paths.

Current-Carrying Capacity: The maximum electrical current that can be carried continuously by a conductor, under specified conditions, without causing objectionable degradation of electrical and mechanical properties of the product.

D

Datum: The theoretically-exact point, axis or plane that is the origin from which the location of geometric characteristics of features of a part are established.

Delamination: A separation between plies within a base material, between a base material and a conductive foil, or any other planar separation within a multilayer printed board. (See also “Blister”.)

Dent: A smooth depression in conductive foil that does not significantly reduce the foil’s thickness.

Design Rule: Guidelines that determine automatic conductor routing behavior with respect to specified design parameters.

Design-Rule Checking: The use of a computer-aided design program to perform continuity verification of all conductor routing in accordance with appropriate design rules.

Design Spacing of Conductors: The spacing between conductors as delineated or otherwise noted on the master drawing.

Design Width of Conductors: The width of conductors as delineated or otherwise noted on the master drawing. (See also “Conductor Spacing”.)

Desmear: The removal of friction-melted resin and drilling debris from a hole wall.

Develop (Phototool): The chemical treatment of radiation-modified photosensitive material in order to produce an image.

Diazo Material: A nonsilver, room-light hardening, ultraviolet-sensitive coating material.

Dielectric: A material with a high resistance to the flow of electrical current.

Dielectric Breakdown: The complete failure of a dielectric material that is characterized by a disruptive electrical discharge through the material that is due to a deterioration of material or due to an excessive sudden increase in applied voltage.

Dielectric Constant: The ratio of the capacitance of a configuration of electrodes with a specific material as the dielectric between them to the capacitance of the same electrode configuration with a vacuum or air as the dielectric.

Dielectric Strength: The maximum voltage that a dielectric can withstand under specified conditions without resulting in a voltage breakdown, usually expressed as volts per unit dimension.

Dimensional Stability: A measure of the dimensional change of a material that is caused by factors such as temperature changes, humidity changes, chemical treatment (aging), and stress exposure.

Dimensioned Hole: A hole in a printed board whose location is determined by physical dimensions or coordinate values that do not necessarily coincide with the stated grid.

Double-Sided Printed Board: A printed board with a conductive pattern on both of its sides.

Drill Diameter: The actual size of the drill body.

E

Edge Spacing: The distance of a pattern or component body from the edges of a printed board.

Effective Permittivity: (See "Dielectric Constant".)

Electrodeposited Foil: A metal foil that is produced by electrodeposition of the metal onto a cathode.

Electrodeposition: The deposition of a conductive material from a plating solution by the application of electrical current.

Electroless Deposition: The deposition of conductive material from an autocatalytic plating solution without the application of electrical current.

Electromagnetic Interference: Unwanted radiated electromagnetic energy that couples into electrical conductors.

Elongation: The increase in length of a material that is caused by a tensile load.

Engineering Drawing: A document that discloses the physical and functional end-product requirements of an item by means of pictorial and/or textual presentations.

Etch Factor: The ratio of the depth of etch to the amount of lateral etch, i.e., the ratio of conductor thickness to the amount of undercut.

Etchant: A solution used to remove the unwanted portion of material from a printed board by a chemical reaction.

Etchback: The controlled removal, to a specified depth, of nonmetallic materials from the sidewalls of holes in order to remove resin smear and to expose additional internal conductor surfaces.

Etched Printed Board: A board having a conductive pattern that was formed by the chemical removal of unwanted portions of a conductive foil.

Etching: The chemical, or chemical and electrolytic, removal of unwanted portions of conductive or resistive material.

External Layer: A conductive pattern on the surface of a printed board.

Extraction Tool: A device used for removing a contact from a connector body or insert, a component from a socket, or a printed board from its enclosure.

F

Fiducial Mark: A printed board artwork feature (or features) that is created in the same process as the printed board conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern or land patterns.

Fillet, Adhesive: The portion of an adhesive that fills the corner, or the angle formed, where two adherents are joined.

Fine-Pitch Technology (FPT): A surface-mount assembly technology with component terminations on less than 0.025" (0.625mm) centers.

First Article: A part or assembly that has been manufactured prior to the start of a production run for the purpose of ascertaining whether or not the manufacturing processes used to fabricate it are capable of making items that will meet all applicable end-product requirements.

Flexible Printed Circuit: A patterned arrangement of printed circuitry and components that utilize a flexible base material with or without a flexible cover lay.

Flexible Printed Wiring: A patterned arrangement of printed wiring that utilizes a flexible base material with or without a flexible cover lay.

Flexible Soldermask: A soldermask that when cured over flexible circuits will not separate, fracture, or delaminate from the surface of the base material, conductors and lands of the coated flexible wiring. IPC-TM-650, TM 2.4.29 specifies a minimum number of 25 cycles using a 0.125" (3.175mm) diameter mandrel.

Flexural Failure: A failure that is caused by the repeated flexing of a material.

Flexural Strength: The tensile strength of the outermost fiber of a material that is being bent.

Foil Lamination: A process for making multilayer printed boards with a surface layer(s) of metal foil bonded in a single operation. (See also "Cap Lamination".)

Foil Profile: The roughness of a foil surface that results from the manufacture of the foil and/or from a bond-enhancement treatment.

Foreign Material (Soldering): A lumpy, irregular coating that has covered, or partially covered, particles of materials that are located on, but are different than, the material or coating of the items to be soldered.

Fork Contact: A type of female connector contact that consists of flat spring metal that has been formed into a two-tine "fork-like" shape so that it mates with a spade contact.

From-To List: Written instructions in the form of a list that indicates the locations of wiring terminations.

Fused Coating: A metallic coating, usually a tin or solder alloy, that has been melted and solidified to form a metallurgical bond to a basis metal.

Fusing: The combining of metals by means of melting, blending and solidification.

Fusing Oil: A thermally stable, non-activated, fluid that is used in the fusing of tin-lead plating on a basis metal. (The application of these predominantly water-soluble fluids is usually preceded by the use of a fusing flux.)

G

Gel Time: The time in seconds required for prepreg to change its physical state from that of a solid material to a liquid, and then back to a solid material.

Gerber Data: A type of data that consists of aperture selection and operation commands and dimensions in X- and Y-coordinates. (The data is generally used to direct a photoplotter to generate artwork.)

Glass Transition Temperature: The temperature at which an amorphous polymer, or the amorphous regions in a partially-crystalline polymer, changes from being in a hard and relatively brittle condition to being in a viscous or rubbery condition.

Global Fiducials: Fiducial marks that are used to locate the position of all of the land patterns on a printed board.

Ground: A common reference point for electrical circuit returns, shielding, or heat sinking.

Ground Plane: A conductor layer, or portion thereof, that serves as a common reference for electrical circuit returns shielding, or heat sinking. (See also "Voltage Plane".)

Ground Plane Clearance: Removed portions of a ground plane that isolate it from a hole in the base material to which the plane is attached. (See Figure 8-8.) shielding or heatsinking (See also "Voltage Plane".)

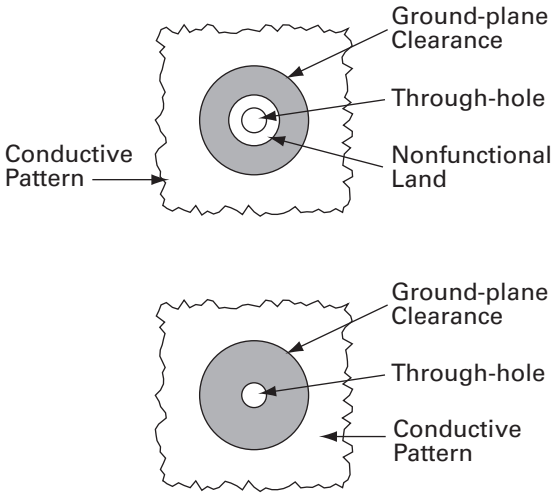


Figure 8-8. Ground Plane Clearance

H

Haloing: Mechanically induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features.

Hand Soldering: Soldering using a soldering iron or other hand-held, operator-controllable apparatus.

Hard Wiring: Electrical wiring that is inseparable from an assembly without the use of special tools and processes.

Heatsink: A mechanical device that is made of a high thermal-conductivity and low specific-heat material that dissipates heat generated by a component or assembly.

Heatsink Plane: A continuous sheet of metal on or in a printed board that functions to dissipate heat away from heat generating components.

Hipot Test: A method in which the unit under test is subjected to a high alternating current (AC) voltage.

Hold-Down Tabs: Conductive tabs extending from the outside of an annular ring or other termination pad used to help secure the pad to the substrate.

Hole Breakout: A condition in which a hole is partially surrounded by a land.

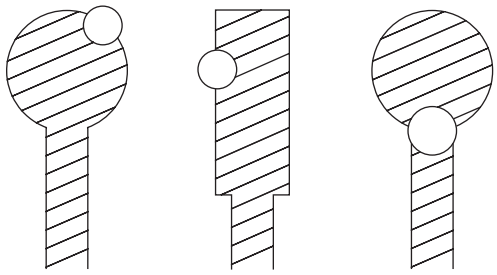


Figure 8-9. Hole Breakout

Hole Density: The quantity of holes in a unit area of printed board.

Hole Location: The dimensional position of the center of a hole.

Hole Pattern: The arrangement of all holes in a printed board with respect to a reference point.

I

Immersion Plating: The chemical deposition of a thin metallic coating over certain basis metals that is achieved by a partial displacement of the basis metal.

Insert (Connector): The element that holds connector contacts in their proper arrangement and electrically insulates the contacts from one another and from the connector shell.

Interlayer Connection: A conductor that connects conductive patterns on internal layers of a multilayer printed board, e.g. a plated-through hole.

Internal Layer: A conductive pattern that is contained entirely within a multilayer printed board.

L

Laminate: A product made by bonding together two or more layers of material.

Laminate Thickness: The thickness of single- or double-sided metal-clad base material prior to any subsequent processing (See also “Board Thickness”.)

Lamination: The process of bonding together two or more layers of material.

Land: A portion of a conductive pattern that is usually used for making electrical connections, for component attachment, or both.

Land Pattern: A combination of lands that is used for the mounting, interconnection and testing of a particular component.

Layer-to-Layer Registration: The degree of conformity of a conductive pattern, or portion thereof, to that of any other conductor layer of a printed board.

Layer-to-Layer Spacing: The thickness of dielectric material between adjacent layers of conductive patterns in a multilayer printed board.

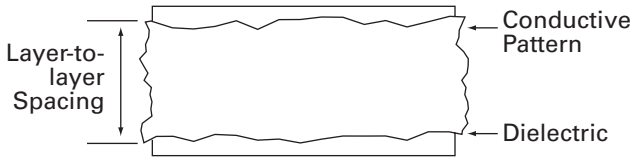


Figure 8-10. Layer-to-Layer Spacing

LPISM: Liquid photo-imagable soldermask.

M

Master Drawing: A document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and nonconductive patterns or elements; the size, type, and locations of holes; and all other necessary information.

Measling: A condition that occurs in laminated base material in which internal glass fibers are separated from the resin at the weave intersection, (this condition manifests itself in the form of discrete white spots or “crosses” that are below the surface of the base material. It is usually related to thermally-induced stress.) (See also “Crazing”.)

Meniscus: The contour of a shape that is the result of the surface-tension forces that take place during wetting.

Metal-Clad Base Material: Base material covered with metal on one or both sides from which conductive patterns may be formed. The material may be rigid or flexible, reinforced or non-reinforced, organic or ceramic.

Metallization: A deposited or plated thin metallic film that is used for it’s protective and/or electrical insulator.

Microsectioning: The preparation of a specimen of a material, or materials, that is to be used in a metallographic examination. (This usually consists of cutting out a cross-section, followed by encapsulation, polishing, etching, staining, etc.)

Microstrip: A transmission-line configuration that consists of a conductor that is positioned over, and parallel to, a ground plane with a dielectric between them.

Minimum Annular Ring: The minimum width of metal(s) at the narrowest point between the edge of a hole and the outer edge of a circumscribing land. (This determination is made to the drilled hole on internal layers of multilayer printed boards and to the edge of the plating on external layers of multilayer and double-sided printed boards.)

Minimum Electrical Spacing: The minimum allowable distance between adjacent conductors, at a given voltage and altitude, that is sufficient to prevent dielectric breakdown, corona, or both, from occurring between the conductors.

Mother Board: A printed board assembly that is used for interconnecting arrays of plug-in electronic modules. (See also "Backplane".)

Mounting Hole: A hole that is used for the mechanical support of a printed board or the mechanical attachment of components to a printed board.

Multilayer Printed Board: The general term for a printed board that consists of rigid or flexible insulation materials and three or more alternate printed wiring and/or printed circuit layers that have been bonded together and electrically interconnected.

Multilayer Printed Circuit Board Assembly: An assembly that uses a multilayer printed circuit board for component mounting and interconnecting purposes.

N

Nail Heading: The flared condition of copper on an inner conductive layer of a multilayer printed board that is caused by hole-drilling.

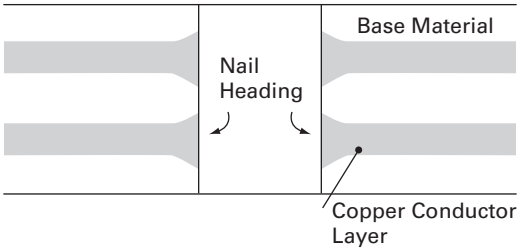


Figure 8-11. Nail Heading

Negative: An artwork, artwork master, or production master in which the pattern being fabricated is transparent to light and the other areas are opaque.

Negative Etchback: Etchback in which the inner conductor layer material is recessed relative to the surrounding base material.

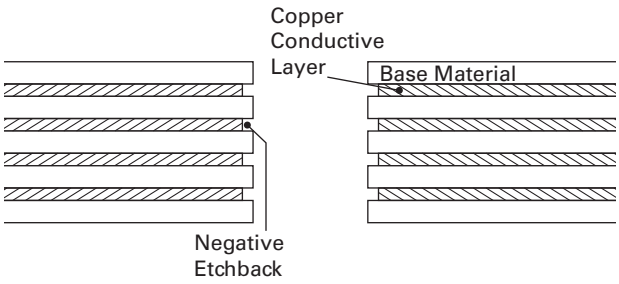


Figure 8-12. Negative Etchback

Net: An entire string of electrical connections from the first source point to the last target point, including land and vias.

Net List: A list of alphanumeric representations, each of which is used to describe a group of two or more points that are electrically common.

Nonfunctional Land: A land that is not connected electrically to the conductive pattern on its layer.

O

Outgassing: The gaseous emission from a printed board or component when a printed board assembly is exposed to a reduced pressure, or heat, or both.

P

Panel: A rectangular sheet of base material or metal-clad material of predetermined size that is used for the processing of one or more printed boards and, when required, one or more test coupons.

Panel Fiducials: Global fiducial marks on a multiple printed circuit board fabrication panel that are not located within the perimeter of an end-product printed board.

Permittivity: A translator fixture plate drilled to match the product under test.

Photoresist: A material that is sensitive to portions of the light spectrum and that, when properly exposed and can mask portions of a base material with a high degree of integrity.

Phototool: A photographic product that is used to produce a pattern on a material. (See also "Artwork" and "Artwork Master".)

Pitch: The nominal center-to-center distance of adjacent conductors. (When the conductors are of equal size and their spacing is uniform, the pitch is usually measured from the reference edge of the adjacent conductors.)

Plated-Through Hole: A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board.

Polarization: The technique of eliminating symmetry within a plane so that parts can be engaged in one way in order to minimize the possibility of electrical, mechanical, or malfunction damage.

Polyimide: A dielectric film material commonly used for flexible circuit fabrication as an insulating layer.

Positional Tolerance: The amount that a feature is pertaining to vary from its true-position location.

Potting Compound: A material, usually organic, that is used for the encapsulation of connectors and wires.

Prepreg: A sheet of material that has been impregnated with a resin and cured to an intermediate stage, i.e., B-staged resin.

Pressfit Contact: An electrical contact that can be pressed into a hole in an insulator or printed board with or without plated-through holes.

Q

Quality-Conformance Test Circuitry: A portion of a printed board panel that contains a complete set of test coupons that are used to determine the acceptability of the board(s) on the board.

R

Registration: The degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product.

Reinforced Adhesive: An adhesive material whose mechanical strength is improved by the addition of glass fibers.

Resin Recession: The presence of voids between the parallel of a plated-through hole and the wall of the hole as seen in microsections of plated-through holes that have been exposed to high temperatures.

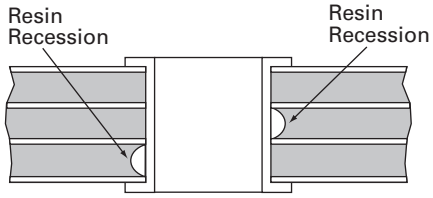


Figure 8-13. Resin

Rigid-Flex Printed Board: A printed board with both rigid and flexible base materials.

S

Sequential Lamination: The bonding process of making a multilayer printed board by multiple laminations of single-sided, double-sided, or multilayer printed board. Sequential lamination may occur one layer at a time or as combinations of multiple layers. The conductive layers are connected by blind, buried or through-hole vias.

Shield: The material around a conductor or group of conductors that limits electromagnetic and/or electrostatic interference.

Signal Conductor: An individual conductor that is used to transmit an impressed electrical signal.

Single-Sided Printed Board: A printed board with a conductive pattern on one of its sides.

Soldermask: A resist that provides protection from the action of solder.

Step-and-Repeat: The successive exposure of a single image in order to produce a multiple-image production master.

Stripline: A transmission-line configuration that consists of a conductor that is positioned equidistant between, and parallel to; ground planes with a dielectric among them.

T

Tenting: The covering of holes in a printed board and the surrounding conductive pattern with a resist that is usually a dry film.

Terminal Pad: A portion of a conductive pattern that is usually used for making electrical connections, for component attachment, or both.

Tetrafunctional Resins: Materials that have four reactive groups per molecule.

Thermal Coefficient of Expansion: See “Coefficient of Thermal Expansion (CTE)”.

Thermal Conductivity: The property of a material that describes the rate at which heat will be conducted through a unit area of the material for a given driving force.

Thermal Expansion Mismatch: The absolute difference between the thermal expansion of two components or materials. (See also "Coefficient of Thermal Expansion (CTE).")

Thermal Relief: The Crosshatching of a ground or voltage plane that minimizes blistering or warping during soldering operations.

Thermoset Adhesive: An adhesive material that undergoes a chemical reaction when exposed to elevated temperatures that leads to it having a relatively infusable or crosslinked state that cannot be softened or reshaped by subsequent heating.

Through-Hole Technology: Techniques used to connect electrical components to a conductive pattern by the use of component holes.

Tooling Feature: A physical feature that is used exclusively to position a printed board or panel during a fabrication assembly or testing process. (See also "Tooling Hole".)

Tooling Hole: A tooling feature in the form of a hole in a printed board or fabrication panel.

True Position: The theoretically exact location for a feature or hole that is established by basic dimensions.

True Position Tolerance: The total permissible deviation from a true position.

U

Unsupported Hole: A hole that does not required plating-through. Most often found in single- and double-sided circuits.

V

Vertical Pins: A type of termination which connects two conductor runs in a solder assembly where the runs are in two different layers.

Via: A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material.

Voltage Plane: A conductor layer, or portion thereof, that serves as a common voltage source at other than ground potential for an electrical circuit, shielding, or heat sinking. (See also "Ground Plane".)

Voltage-Plane Clearance: Removed portions of a voltage plane that isolate it from a hole in the base material to which the plane is attached.

Industry Specifications

Following is a listing of the commercial and federal specifications for the manufacture and testing of flexible and rigid-flex circuits. They may be used in connection with this Design Guide.

Federal

DOD-STD-100	Engineering drawing practices
MIL-C-14550	Electroplated Copper
MIL-P-81728	Electroplated tin/lead
MIL-F-14256	Flux, soldering liquid (resin based)
MIL-G-45204	Gold plating, electro-deposited
MIL-I-46058	Electrical insulating compound (for coating printed circuit assemblies)
MIL-P-50884	Specification for flexible and rigid-flex printed wiring
MIL-P-13949	Plastic sheet, laminated - metal clad
MIL-STD-105	Sample procedures & tables for inspection attributes
MIL-STD-275	Printed wiring for electronic equipment
MIL-STD-202	Test methods for electronic and electrical component parts
MIL-STD-454	Standard general requirements for electronic equipment
MIL-STD-810	Environmental test methods
MIL-STD-2118	Design requirements for flexible and rigid-flex printed wiring
QQ-S-571	Solder, tin alloy
QQ-C-576	Copper flat products

IPC

IPC-T-50F	Terms and definitions
IPC-MF-150	Copper foil for printed wiring applications
IPC-FC-231	Flexible bare dielectrics for use in flexible printed wiring
IPC-FC-232	Specifications for adhesive coated dielectric films for use as cover sheets for flexible printed wiring
IPC-FC-241	Metal-clad dielectrics for use in fabrication of flexible printed circuits
IPC-D-300	Printed board dimension and tolerances
IPC-A-600	Acceptability of printed boards
IPC-SM-840	Qualification and performance of permanent polymer coating (solder mask) for printed boards

IPC-2221	Generic standard on printed board design (Supersedes IPC-D-275)
IPC-2222	Sectional design standard for rigid organic printed boards (Supersedes IPC-D-275)
IPC-2223	Secional design standard for flexible printed boards (Supersedes IPC-D-249)
IPC-2224	Sectional standard for design of PWBs for PC cards
IPC-2225	Sectional design standard for organic multichip modules (MCM-L) and MCM-L assemblies
IPC-4101	Laminate/Prepreg materials standard for printed boards (Supersedes IPC-L-108, IPC-L-109, IPC-L-112, IPC-L-115, and IPC-AM-361)
IPC-6011	Generic performance specification for printed boards (Supersedes IPC-RB-276)
IPC-6012	Qualification and performance specification for rigid printed boards (Supersedes IPC-RB-276)
IPC-6013	Gualification and performance specificaiton for flexible printed boards (Supersedes IPC-RF-245 and IPC-FC-250A)
IPC-6015	Qualification and performance specification for organic multichip module (MCM-L) mounting and interconnecting structures
J-STD-001B	Requirements for soldered electrical and electronic assemblies
J-STD-002A	Solderability tests for component leads, terminations, lugs, terminals and wires (relpaces IPC-S-805)
J-STD-003	Solderability tests for printed boards (replaces IPC-S-804A)
J-STD-004	Requirements for soldering fluxes - (includes Amendment 1)

Application for copies of IPC specifications should be addressed to:

Institute for Interconnecting and Packaging Electronic Circuits
7380 North Lincoln Ave.
Lincolnville, IL 60646

Commercial

UL-794	Certification standard

Teledyne Electronic Technologies
Printed Circuit Technology Business Unit

110 Lowell Road, CS 68

Hudson, New Hampshire 03051

Tel: (603) 889-6191

Fax: (603) 882-4457

Email: sales@tetpct.com

TELEDYNE ELECTRONIC TECHNOLOGIES

Printed Circuit Technology Business Unit

110 Lowell Road, CS 68, Hudson, New Hampshire 03051
Tel: (603) 889-6191 • Fax: (603) 882-4457

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