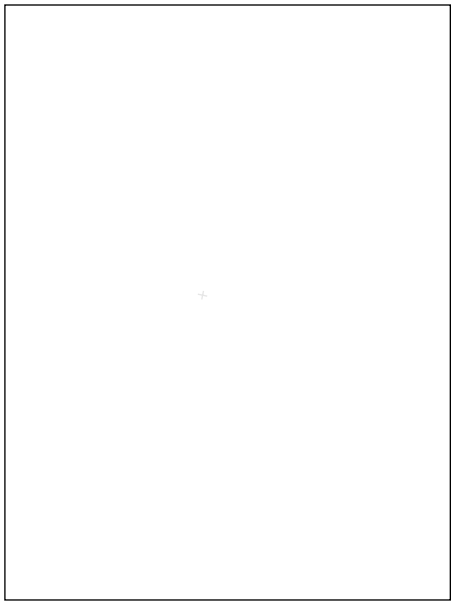
PM-2060i Family
User’s Guide

PM-2060i Family User's Guide

Preliminary



PM-2060i; PM-2040i; PM-2020i; PM-2010i ImageChip Printer/Multifunction Enhancement ASICs

Pixel Magic, Inc.

UG-2060-1.A
March, 1999

COPYRIGHT/TRADEMARK NOTICE

Pixel Magic, Inc.
300 Brickstone Square
Andover, MA 01810
VOICE: (978) 470-8830
FAX: (978) 470-8892
WEB: www.pixelmagic.com

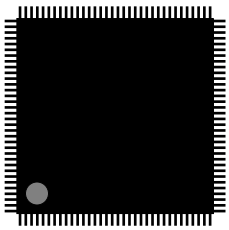
•

Pixel Magic, Inc. — Japan
Oak Technology, K.K.
Musashino Nissay Plaza 5F
1-11-4 Nakamachi Mushashino City
Tokyo 180 Japan
VOICE: +81-422-56-3761
FAX: +81-422-56-3778

•

Pixel Magic, Inc. — Taiwan
Oak Technology, Inc.
Room B, 7F, No. 370
Section 1, Fu Hsing South Road
Taipei, Taiwan R.O.C.
VOICE: 886-2-784-9123
FAX: 886-2-706-7641

Table of Contents



Preface

This user's guide describes how to use the PM-2060i family of Printer/Multifunction Enhancement ASICs.

Manual Organization

The organization of this manual is as follows:

Chapter: 1 Functional Description and Specifications

This chapter describes the functionality and features of the PM–2060i and the chip's electrical and environment specifications.

Chapter: 2 PM-2060i Signal Descriptions

This chapter provides a complete description of the PM-2060i's signal pins.

Chapter: 3 Source Data I/O

This chapter describes the two source data input ports of the PM-2060i, and the overall system clock requirements for data transfer.

Chapter: 4 PM-2060i Interface Modes

This chapter describes the PM-2060i's interface modes used for transactions into and out of the chip. Information on initialization power and grounding concerns, and the Contone Auto Positioning Mode are included.

Chapter: 5 PM-2060i Register Descriptions

This chapter describes each of the PM-2060i's registers and all its fields. These descriptions include information that is essential for programming the PM-2060i.

Chapter: 6 PM-2060i Timing Diagrams

This chapter presents the AC timing diagrams for all data transactions on the PM-2060i.

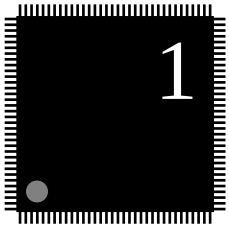
Chapter: 7 PM-2060i Package Information

This chapter provides information about the PM-2060i package, including its dimensions, pin characteristics, and pin locations.

Manual Conventions

The following conventions apply throughout this manual:

- Register names appear in boldface type (for example, **CONTROL REGISTER A**).
- The name of a signal pin that is asserted active high appears in boldface type (for example, **OFRDY**).
- The name of a signal pin that is asserted active low appears in boldface type with an overline (for example, $\overline{\textbf{OE}}$).
- Bit widths and pin numbers of signal pins are expressed as **PIN**[Max:Min], so the command port is expressed as **CD**[15:0].
- HEXADECIMALS: the prefix “0x” is used to indicate a hexadecimal literal value.
- 2060i or PM-2060i is used to refer to all members of the PM-2060i family of ImageChips, unless specifically noted otherwise.



Functional Description and Specifications

This chapter describes the functionality and features of the PM-2060i and the chip's electrical and environment specifications.

Table of Contents

1.1 Functional Description

The PM-2060i ImageChip family of Printer/Multifunction Enhancement ASICs is a single-chip implementation for providing state-of-the-art resolution enhancement of text, line art, and photographic images for laser-based products including printers, multifunction devices, high-speed workgroup devices, and digital laser copiers. The ImageChip provides resolution enhancement for printing, fax printing, and 2x high-resolution rendering. The PM-2060i also supports 256 shade, 8-bit data for Multi-bit (contone) modes. It operates on a single +3.3 V nominal power supply and its I/Os are 5 V tolerant.

The ImageChip supports a number of operating modes and features depending on the specific model. Refer to Table 1-1 for a summary of the features supported by each model in the PM-2060i family. Font-independent edge enhancement of all text and line art graphics provides more than doubled effective horizontal and vertical resolution eliminating jaggies. The ImageChip will print 100, 200, 300, or 600 dpi source data on a typical 600 dpi engine. A 2x high resolution rendering mode provides the ability to accept 2x source data, rendering 1200 dpi quality on a 600 dpi engine. This feature allows 600 dpi printers to directly compete with 1200 dpi printers.

Integration of the ImageChip into a serial video printer engine design is simple and straightforward, since the ImageChip can operate on the serial video data directly. A parallel video data interface is provided for higher-speed applications. Internal, downloadable engine calibration tables allow the enhancement to be optimized for different manufacturers' laser print engines and scanners. Utilizing years of engineering, laboratory, and production experience in optimizing numerous laser print engines, Pixel Magic output directly drives the engine video.

The functional block diagram of the ImageChip is shown in Figure •. It consists of a 1) data source multiplexer, 2) Line Store memory, 3) two enhancement processors, 4) dual 256 x 10 calibration LUT memory, 5) pulse position LUT memory, 6) digital modulator, 7) processor interface, 8) margin control logic, and 9) clock divider. Each of these blocks is described below. All data and descriptions assume a 600 dpi print engine, unless specifically noted otherwise.

PM-2060i PRODUCT LINE				
Features/Model	**PM-2060i**	**PM-2040i**	**PM-2020i**	**PM-2010i**
Max. Pages Per Minute (ppm)	60	40	20	10
Max Line Length @ 600dpi (in)	13.65	11.7	8.25	8.25
300dpi Edge Enhancement	Yes	Yes	Yes	Yes
600dpi Edge Enhancement	Yes	Yes	Yes	Yes
Fax Edge Enhancement	Yes	Yes	Yes	Yes
1200dpi Rendering	Yes	Yes	Yes	Yes
Contone Rendering Mode	Yes	Yes	NO	NO
Contone Auto Position Mode	Yes	Yes	NO	NO
Economy Mode	Yes	Yes	Yes	Yes
Serial Data Input Mode	Yes	Yes	Yes	Yes
Parallel Data Input Mode	Yes	Yes	Yes	Yes
Beam Detect Synchronization	Yes	Yes	Yes	Yes
On-chip Digital Modulator	Yes	Yes	Yes	Yes
3.3 Volt Supply (5V I/O tolerant)	Yes	Yes	Yes	Yes
Package – PQFP (pins)	52	52	52	52
Max Video Rate (MHz)	66	50	30	15
Min Video Rate (MHz)	3	3	3	3

Table 1-1

1.1.1 PM-2060i Processing Features

Major features of the PM-2060i family include the following:

- Text and Line Art Edge Enhancement
  - Source Data at 1/6x, 1/3x, 1/2x, or 1x of Engine Resolution (DPI)
  - Fax Enhancement at 200 DPI Source Data
- 2x Rendering Mode
- Multi -Bit (contone) Mode (PM-2060i, PM-2040i only)
  - Grayscale mode suitable for Digital Copy or Grayscale PDL
  - Direct 8-Bit Data Path at 300 or 600 DPI
  - 256 Gray Levels
- Contone Auto Position Mode (PM-2060i, PM-2040i only)
- Continuous Print Mode Supports Infinite Page Length
- Two Source Data Input Modes
  - 1-bit Serial
  - 8-bit Parallel
- Precision Internal Digital Modulator
  - 66 MHz Maximum Video Rate
  - 3 MHz Minimum Video Rate
- Multiple Print Engine Support — 300 to 800 DPI
- Internal Beam Detection Synchronization
- Serial or Parallel CPU Interface Options
  - 12-Pin Multiplexed Parallel Interface with Endian Control
  - 2-Pin Serial Interface
  - Big Endian or Little Endian Programmable
- Internal Line Store Memory Supports the following Line Lengths at 600 DPI.
  - PM-2060i = 13.65"
  - PM-2040i = 11.7"
  - PM-2020i = 8.25"
  - PM-2010 = 8.25"

- Economy Print Mode
- +3.3 V Power Supply
- 52-Pin Metric Plastic Quad Flatpack (PQFP) Package
- Internal LUT for print engine calibration
- Margin control

1.1.2 General Interface Requirements

The interface requirements to the ImageChip are minimal. In the parallel CPU interface mode, two-bit address, 8-bit data bus, **CHIP SELECT**, **READ**, **WRITE**, and **RESET** control lines constitute the CPU interface; the ImageChip provides Line Sync (**LSYNC**), End Of Page (**EOP**), and Video Clock for video source. In the serial CPU interface mode, bit 0 of the data bus is the serial CPU data line, and bit 1 of the data bus is the serial CPU clock line.

The printer engine interface supplies **BEAM DETECT** and **FSYNC** (Vertical Sync). The ImageChip provides the enhanced serial video to the printer engine.

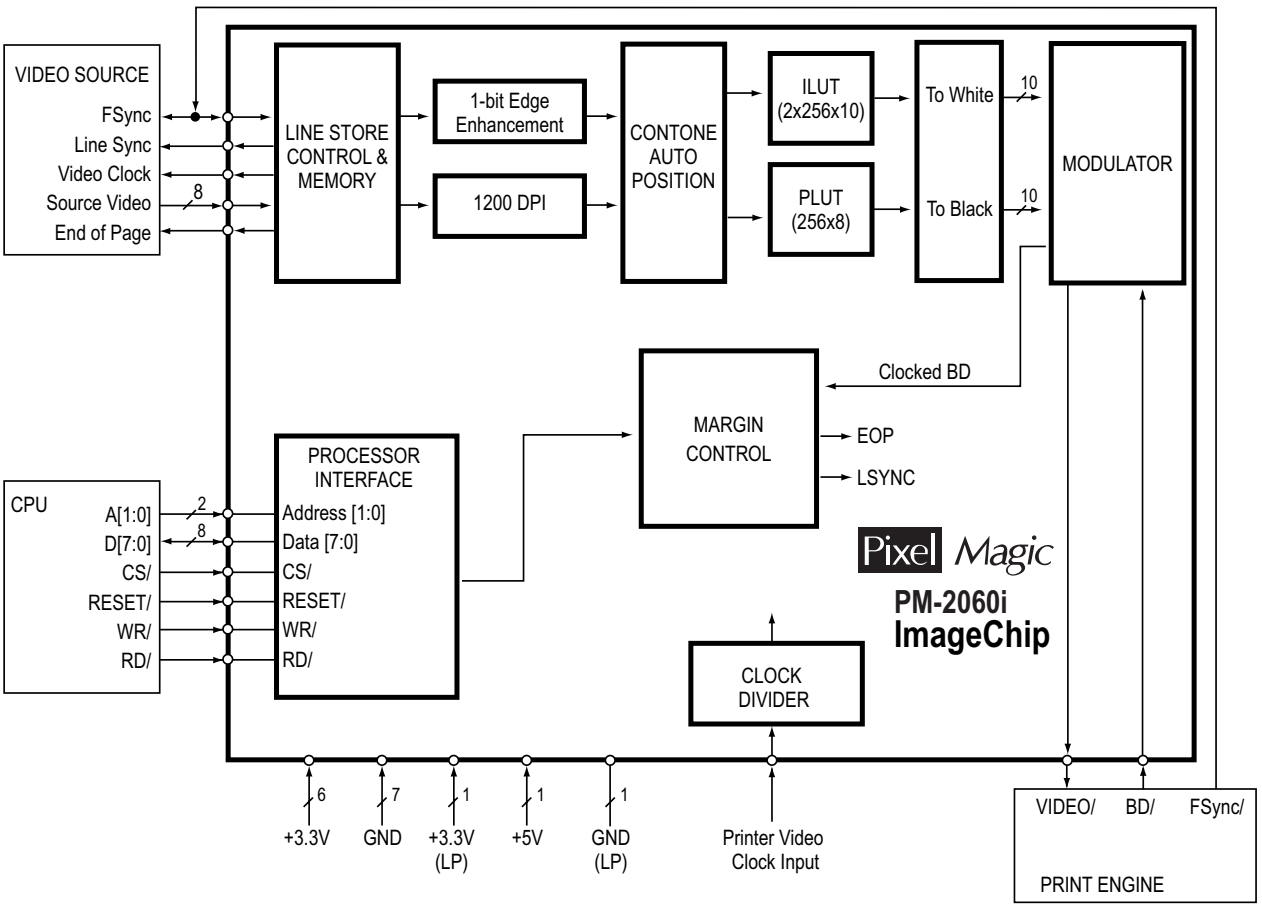


Figure 1-1. PM-2060i Block Diagram

The nominal power supply for the ImageChip is +3.3 V. A ground plane is highly recommended, as are bypass capacitors on each VDD pin.

1.1.3 Functional Units

The PM-2060i integrates the following functional units, illustrated in Figure 1-1:

- **Data Source Multiplexer**

The video source data to the ImageChip is fed into a 8-bit source data input in the parallel source data mode. In the serial source data mode, bit 0 of the 8-bit source data input accepts serial video data. The ImageChip provides a source video clock. The choice of data format is dependent on the interface options of the CPU and the bandwidth requirements of the printer.

- **Line Store Memory**

The on-chip line store memory is 16-bit SRAM. The function of the line store memory is to provide storage of multiple scan lines in the format required by the enhancement modules. The line store memory must store source data for 200, 300, 600, or 1200 dpi scan line lengths. The re-configuration of the line store memory for each of the enhancement modes is automatic, and therefore transparent to the user. The only restriction to the user is that the scan line length is limited to the maximums shown below at 600 dpi:

Model	Maximum Line Length
PM-2060i	13.65"
PM-2040i	11.7"
PM-2020i	8.25"
PM-2010i	8.25"

- **Enhancement Processors**

The Edge, Multi-Bit, 1200DPI, and Grayscale Enhancement processors provide the ImageChip with its primary image and text enhancement functions.

Edge Enhancement — Font-independent text and line art graphics are both enhanced by more than doubling their effective vertical and horizontal resolution. Source data can be equal to, one-half, one-third, or one-sixth of the print engine resolution. For a 600 dpi engine resolution, the ImageChip will enhance 200, 300 or 600 dpi source data. The edge enhancement logic determines the additional and fractional dots needed to eliminate the “jaggies” so the effective resolution is doubled. A 9 x 10 window is used to generate the dot position information to the on-board modulator.

High Resolution Rendering — The ImageChip features the ability to accept 2x source data, and render 1200 dpi quality print on a 600 dpi engine. This allows the 600 dpi printer to compete with 1200 dpi printers.

Grayscale Rendering (PM-2060i, PM-2040i only) — Eight-bit or four-bit data is accepted for grayscale printing with 256 or 16 shades per pixel, respectively. Three screening options are available for this grayscale path — 600 x 600, 300 x 300, and 300 x 150. This data path may be used for any grayscale image data such as from a scanner in digital copy applications, or printing grayscale information directly from a PDL.

Contone Auto Position (PM-2060i, PM-2040i only) — 600 x 8 or 600 x 4 data is enhanced by detecting solid black and white areas, and automatically positioning varying width pulses adjacent to solid blacks to improve anti-aliased text, line art and halftone dots.

- **Internal Calibration LUT (ILUT) Memory**

The internal calibration LUT (**ILUT**) memory is a 2 x 256 x 10 memory used to store the print engine calibration tables that provide the correction necessary to compensate for print engine, toner, paper, and environmental variables in the printing process. The **ILUT** is addressed and downloaded directly by the CPU at power up. Special data may also be downloaded to the **ILUT** to implement Toner Saver functions. Different tables can be loaded between planes for color printing. The **ILUT** contents may be read by the CPU. The data for the **ILUT** is provided by Pixel Magic for the particular laser printer engine.

- **Position LUT (PLUT) Memory**

The position LUT (**PLUT**) memory is a 256 x 8 memory used to modify pulse position data for the digital modulator. Under normal operating conditions, the table is loaded with unity data (no position modification takes place; data supplied by Pixel Magic). Please consult Pixel Magic for detailed information regarding the use of the **PLUT** memory.

- **Digital Modulator**

The precision digital modulator features precision pulse width and position control enabling superior edge and photo enhancement. Placement of laser beam transitions is located to within $1/1024^{th}$ of the engine clock. The start of each line scan is synchronized to the beam detect signal to within $1/256^{th}$ of a video clock period to minimize line jitter and optimize print quality. The modulator output directly drives the engine video. In most cases, the modulator requires no external components. An external buffer/driver chip may be needed depending on the line impedance and the physical lead length to the laser diode driver.

- **Processor Interface**

The processor interface can be configured as either 8-bit parallel or serial. This is accomplished by selecting the logic state of the **WR** pin when the 2060i is reset. When in parallel mode, the interface consists of an 8-bit data bus, a 2-bit address bus, and three control lines – **CHIP SELECT**, **WRITE**, and **READ**. In the serial mode, the interface consists of the two LSBs of the data bus, with DATA(0) acting as the serial data line, and DATA(1) acting as the serial clock line.

- **Margin Control Logic**

The 2060i ImageChip provides 16-bit registers for left and top margins, line length and number of lines. The margin control logic uses these registers with **FSYNC** and the clocked Beam Detect signals to produce both internal signals that control the printable horizontal and vertical areas of the page, and external **LSYNC** and **EOP** (end of page) signals.

- **Video Clock Divider**

An external oscillator provides Video Clock to the 2060i ImageChip, at a frequency equal to (1x) or a multiple of (2x, 4x, or 8x) the native engine pixel rate. The Clock Divider circuit internal to the ImageChip must be programmed by software (via Control Register B) for the appropriate divider, so that, regardless of the video clock frequency input, the divider output is at the video pixel rate. The maximum video clock input is 66 MHz for either the parallel or serial input modes. When using the parallel data input mode, the clock input need only be 1x (with the divider set for divide-by-1), although higher speed choices are also fine such as 2x, 4x, or 8x (with the divider set for divide-by-2, 4, or 8, respectively).

The serial data input mode places additional restrictions on the video clock frequency. Since the serial data mode only transfers one bit of data per clock period, the ImageChip requires a clock input fast enough to match the input data to the print engine. Therefore, depending on the bit depth of the data, either a 4x or 8x clock must be provided to the ImageChip, and the Clock Divider must again be programmed to divide by that same multiplier to provide an internal clock rate equal to the video pixel rate. For example, if the printer has a 10 MHz pixel clock (the 600 DPI rate), then the 1200 DPI serial data (4 times the data) must be transferred at 40 MBits per second. This transfer rate through the serial interface requires a 40 MHz clock, and the clock divider must be set to divide-by-4 (for all modes). The 300 grayscale mode also requires a 4x clock when using the serial data mode; the 600 grayscale mode requires an 8x clock for the serial data mode. This limits the speed of the printer that the ImageChip can support using the serial data input mode (66 MHz maximum clock rate). Controllers designed for faster printers and high resolution printing should therefore use the parallel data input mode.

- **Color Printing**

The ImageChip is designed to be used in both monochrome and color print engines. The various print modes, precision modulator, and laser beam control provided by the ImageChip will fully support color printing. In CMYK four-color printing applications, each color plane is processed separately. The ImageChip provides complete programming flexibility by allowing the look-up tables (LUT) to be loaded with different values and the functional mode to be changed (edge enhancement on/off, etc.) between processing planes; edge enhancement can be turned "on" for the black (K) plane only, for example. The internal screening (single-bit enhancement or multi-bit screen options) may be used to produce color prints or, if desired, the internal screening may be turned off and the user can provide a unique screen. The ImageChip programming flexibility provides the controller designer with a wide latitude of design alternatives for both monochrome and color printing.

1.2 ELECTRICAL SPECIFICATIONS

The following table provides the recommended operating conditions for interfacing to the ImageChip. Please note that while the ImageChip is made up exclusively of low-voltage chip interface circuits, all I/O's (i.e. input only, tri-state, or bi-directional) are 5 Volt tolerant, that is, these pins can be connected to buses which can swing between 0 V and 5 V.

ABSOLUTE MAXIMUM RATINGS				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Supply Voltage	V_{DD}	-0.3	+7.0	Volts
Input Voltage		-0.3	V_{DD}+0.3	Volts
Input Current	I_{IN}	-10	+10	mA
Storage Temperature		-40	+125	°C

Table 1-2

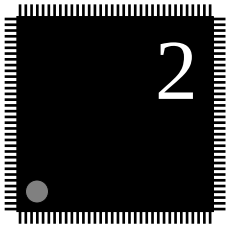
ELECTRICAL SPECIFICATIONS				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Nominal Supply Voltage	V_{DD}	3.15	3.45	Volts
5.0 Volt Reference Level*	V_{DD5}	4.75	5.25	Volts
Power Consumption at 75 MHz, +3.6 V	P_D	—	TBD	Watts
Ambient Operating Temperature	T_{AO}	0	+70	°C

*V_{DD5} is connected to the system's 5 V supply to provide 5 V tolerance on I/O signal pins. In systems where 3.3 V signaling only is used, connect V_{DD5} to a 3.3 V supply.

Table 1-3

DC CHARACTERISTICS, V_{DD} = 3.3V, T= 0°C to 70°C				
Parameter	**Conditions**	**Min.**	**Max.**	**Unit**
Input Low Voltage	—	—	0.8	Volts
Input High Voltage	—	2.0	—	Volts
Output Low Voltage	I_{OL} = 8 mA	—	0.4	Volts
Output High Voltage	I_{OH} = 8 mA	2.4	—	Volts
Input Current	—	—	10	µA
Input Capacitance	—	—	5	pF

Table 1-4



PM-2060i Signal Descriptions

This chapter provides a complete description of the PM-2060i's signal pins.

Table of Contents

2.1 Signal Pin Descriptions

This section provides detailed descriptions of the PM-2060i signal pins.

2.1.1 Source Video Interface

Parallel Video Data Input **Pins 52 (MSB),1, 2, 3, 4, 7, 10, 11 (LSB)**

8-bit parallel video data input; selected by a 00 on bits 12-11 in Control Register A.

Video Source Clock Output **Pin 44**

This clock output latches video data at video input pin(s) into the ImageChip. It may be programmed to be either rising or falling edge triggered by Control Register C, Bit 9.

Serial Video Data Input **Pin 11**

Serial video data input; selected by a 11 on bits 12-11 in Control Register A.

2.1.2 CPU Address, Data and Control

$\overline{\text{Chip Select}}$ Input **Pin 12**

Selects the ImageChip; active low.

$\overline{\text{WR}}$ Input **Pin 41**

Write signal for Internal Register, Line Store Memory, and LUTs; active low. Also used to select parallel or serial CPU interface; used in conjunction with **$\overline{\text{RESET}}$** (See *Processor Mode Control* below, and *ImageChip/Processor Interface* sections.)

$\overline{\text{Reset}}$ Input **Pin 21**

Resets the ImageChip to initial power-up state; active low. Also used to select parallel or serial CPU interface; used in conjunction with **$\overline{\text{WR}}$** (See *Processor Mode Control* below, and *ImageChip/Processor Interface* sections.)

Address Inputs **39 (MSB), Pins 38 (LSB)**

Address lines for accessing all control registers and internal memories. The state of the two address lines determines which of the following are accessed — the high order byte of the internal address register (00), the low order byte of the internal address register (01), or the internal 8-bit data register (10) which will contain the internal data addressed by the internal address register. A fourth access mode (11) accesses the internal 8-bit data register which will contain the internal data addressed by the internal address register with auto-increment of the address register.

Data Bidirectionals **Pins 37 (MSB), 30-25, 22 (LSB)**

Data lines for writing and reading data to/from all control registers and internal memory.

$\overline{\text{RD}}$ Input **Pin 40**

Enables read data onto CPU DATA bus for read cycles. Act an output enable.

Clock Input **Pin 49**

Clock input; rising edge triggered; 66 MHz maximum input frequency. Input frequency is dependent on the operating mode of the ImageChip.

2.1.3 Processor Mode Control

$\overline{\text{WR}}$ Input **Pin 41**

If sampled high at the end of a reset, the processor interface is 8-bit multiplexed asynchronous. The address, data and control lines all function as described in the *CPU Address, Data and Control* section. If sampled low at the end of a reset, the processor interface is bit serial. **DATA**[1] (pin 25) becomes the serial clock, and **DATA**[0] becomes the serial data line.

2.1.4 Synchronization

LSync Output **Pin 42**

Output timing reference derived from **BEAM DETECT**. **$\overline{\text{LSYNC}}$** output is used to indicate the start of a line with data transfers. **$\overline{\text{LSYNC}}$** will always occur at the start of each line before any **SOURCE CLOCK OUTPUT**. UG-2060-1.A output polarity can be programmed by Control Register C, Bit 8.

End of Page (EOP) Output Pin 13

This signal defines the printable area of the page. This pin may be programmed for active high or low by Control Register C, Bit 7. **EOP** goes true at the start of the first printable line, and goes false at the end of the last printable line.

2.1.5 Printer Engine Interface

FSync Input Pin 14

FSync is the frame synchronization signal from the printer engine which signifies the start of a new page. FSync initiates vertical margin line counting and subsequent data transfer. The edge used to start the timing sequence is controlled by Control Register C, Bit 6. Regardless of the polarity of the **FSYNC** input pulse, if this control register bit is set to "1", the rising edge of the **FSYNC** pulse is used as the start of page; when this control register bit is set to "0", the falling edge is used as the start of page. On reset, this register defaults to the falling edge active. The **FSYNC** pulse width must be a minimum of two periods of the **CLOCK INPUT**.

Beam Detect Input Pin 33

BEAM DETECT (BD) signal from printer engine. Used as timing reference for data transfer to printer engine. The edge used to start the timing sequence is controlled by Control Register C, Bit 5. If this control register bit is set to "1", the falling edge is used; when this control register bit is set to "0", the rising edge is used. The BD pulse width must be a minimum of two periods of the **CLOCK INPUT**.

Video Output Pin 36

Video output signal to printer engine laser diode driver. The polarity of the video output data may be programmed by Control Register C, Bit 12. When Bit 12 is set to logic "1", the output is normal video, with logic "0" as white data. When Bit 12 is set to logic "0", the output is reversed video, with logic "1" as white data. The video output may be enabled by Control Register C, Bit 13.

2.1.6 Power and Ground

VDD3 Pins 5, 6, 18, 31, 32, 45

All VDD pins connect to +3.3 V nominal power supply, and should be bypassed to ground as close as possible to the pin with a 0.1µF capacitor.

VSS Pins 8, 9, 20, 34, 35, 47, 48

All VSS pins connect to the system ground plane.

VDD5 **Pin 19**

VDD5 connects to +5 V nominal power supply.

LPVDD **Pin 24**

LPVDD connects to +3.3 V nominal power supply, and should be bypassed to ground as close as possible to the pin with 0.1µF, 0.01µF, and 10µF capacitors.

LPVSS **Pin 23**

LPVSS connects to the system ground plane.

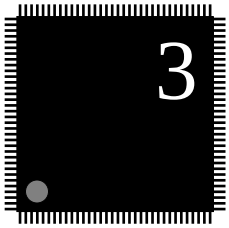
2.1.7 Other

Test **Pin 15, 16, 17**

Pin 15, 16, 17 must be grounded for proper operation of the ImageChip.

UNUSED **Pins 51, 50, 46, 43**

These pins must be pulled high to +3.3 V through 4.7 kOhm resistors for proper operation of the ImageChip.



Source Data I/O

This chapter describes the source data input port of the PM-2060i, and the overall system clock requirements for data transfer.

Table of Contents

3.1 Data Input Port

The 2060i ImageChip can accept video data from two sources: parallel data at the **PARALLEL VIDEO INPUT** pins (52, 1-4, 7, 10, and 11); or serial data on the **SERIAL VIDEO INPUT** pin (11), in conjunction with the **VIDEO SOURCE CLOCK OUTPUT** pin (44). The video data source is controlled by Control Register A, Bits 12:11.

3.2 SOURCE DATA TRANSFER

Data transferred to the ImageChip must be transferred at such a rate as to maintain the video output rate required by the print engine. The operating mode being used will determine the required data transfer rate. The data transfer is synchronized with the laser scan.

The maximum video clock rate at the output of the ImageChip is 66 MHz (PM-2060i), 50 MHz (PM-2040i), 30 MHz (PM-2020i), and 15 MHz (2010i). In the parallel transfer mode there are no limitations. When operating in the serial mode however, the 600 x 8 and 300 x 8 multi-bit modes and the 1200 x 1 one-bit mode, all limit the speed at which the ImageChip can provide data to the printer.

In parallel mode, the ImageChip is able to clock in 8-bits, or a byte, of data. This allows the burst transfer rate to be less than the video rate. For example, in 600 x 1 mode, since 8-bits can be transferred, the burst transfer rate would be 1/8th the video rate.

OPERATING MODE E.G.*	**PARALLEL DATA TRANSFER RATE**	
Single-bit data		
1200 x 1	1/2 the video rate	33 MHz
600 x 1	1/8th the video rate	8.25 MHz
300 x 1	1/16th the video rate	4.125 MHz
200 x 1	1/24th the video rate	2.75 MHz
Multi-bit data (PM-2060i and PM-2040i only)		
600 x 8	video rate	66 MHz
300 x 8	1/2 the video rate	33 MHz
600 x 4	1/2 the video rate	33 MHz

**E.G. 66 MHz 600 DPI Printer & PM-2060i*

Another advantage to the parallel mode is that data transfer only needs to occur in the printable area of the page. In other words, no data transfer takes place in the margin areas, whereas in serial mode, white data must be sent in these areas.

Also note that when operating in modes where the data resolution is less than that of the printer engine resolution, data transfer does not take place during every scan line. For example, on a 600 dpi printer engine, in mode 4 (300 x 1), data transfer will occur every other scan line since the second line would be a duplicate of the first.

In the serial mode, the peak engine video rate is 66 MHz (PM-2060i), 50 MHz (PM-2040i), 30 MHz (PM-2020i), and 15 MHz (2010i). The peak serial bit transfer rate is also 66 MHz. In the 8-bit modes, the PM-2060i and PM-2040i need eight bits of information for each video clock; since the chip can only clock one bit of information on each clock, eight clocks are required to get one byte of information. This then limits the operating clock frequency to one-eighth of the 66 MHz maximum, or 8.25 MHz. In the 1200 x 1 bit mode, the PM-2060i family requires four times the amount of data for each video clock; this then limits the operating clock frequency to one quarter of the maximum video rate, or 16.5 MHz for the PM-2060i, 12.5 MHz for the PM-2040i, 7.5 MHz for the PM-2020i, and 3.75 MHz for the PM-2010i.

3.3 Source Video Input Modes

The source video data can be transferred to the ImageChip as either 8-bit parallel or serial data. Each interface option is described below.

3.3.1 Parallel Mode

With Control Register A, Bits 12:11 set to 00, the parallel source video interface is selected. The interface consists of the 8-bit **PARALLEL VIDEO DATA INPUT**, **VIDEO SOURCE (VS) CLOCK OUTPUT**, and **LSYNC**. The LSync output is used to indicate the start of a line with data transfer.

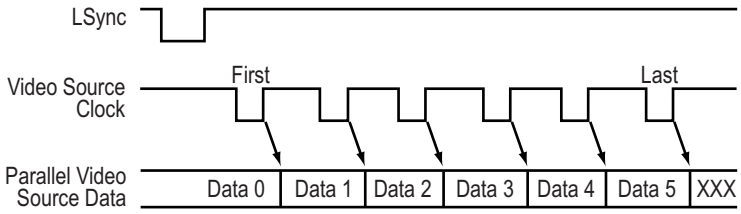


Figure 3-1

As shown in Figure 3-1, the parallel video data is clocked on the rising edge of each **VS CLOCK** transition. The parallel video data must meet the required setup time to the next rising edge of the **VS CLOCK**. The first **DATA** for each line must be valid *before* the first **VS CLOCK**; i.e. the data must be "primed" for the start of each line. **LSYNC** will always occur at the start of each line before any **VS CLOCK** pulses. **LSYNC** may be programmed to be active low or high (low is shown in the figure). **VS CLOCK** may be programmed to be rising or falling edge triggered (rising edge shown in the figure).

There is a pipeline priming feature in the PM-2060i ImageChip that primes the external source data device if needed. It can provide up to seven (7) prime clocks at the start of each page. After **FSYNC** is asserted, the 2060i will issue **VS CLOCK** pulses to prime the external data source. The value N is programmed in the **PRIME** Register. The prime clocks are issued after **FSYNC** only following a write to the **PRIME** Register; it is therefore possible to prime once at the beginning of a set of pages for multi-color print jobs.

3.3.2 Serial Mode

With Control Register A, Bits 12:11 set to 11, the serial source video interface is selected. The interface consists of the **SERIAL VIDEO DATA INPUT**, **VIDEO SOURCE (VS) CLOCK OUTPUT**, and **LSYNC**. The **LSYNC** output is used to indicate the start of a line with data transfer. **VS CLOCK** output is continuous and free running.

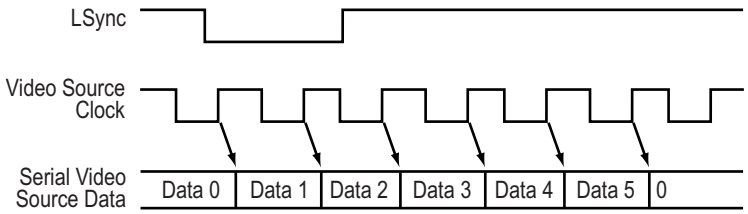
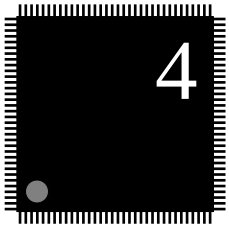


Figure 3-2

As shown in Figure 3-2, the serial video data is clocked on the rising edge of each **VS CLOCK** transition. The serial video data must meet the required setup time to the next rising edge of the **VS CLOCK**. The first DATA for each line must be valid **BEFORE** the first **VS CLOCK** after **LSYNC** goes low; i.e. the data must be "primed" for the start of each line. The serial data must wait for the first rising edge after **LSYNC** goes low to start clocking data. The source video data must contain the margin padding data. **LSYNC** may be programmed to be active low or high (low is shown in the figure). **VS CLOCK** may be programmed to be rising or falling edge triggered (rising edge shown in the figure). **VS CLOCK** is always a free-running clock.



PM-2060i Processor Interface Modes

This chapter describes the PM-2060i's processor interface modes used for transactions into and out of the chip. Information on initialization power and grounding concerns.

Table of Contents

4.1 INTERFACE MODES

The PM-2060i ImageChip family processor interface can be configured as either an 8-bit parallel or serial interface. The processor mode is changed by performing a **RESET** with the **$\overline{\text{WR}}$** signal held at the appropriate logic level to select the interface mode desired — held high at the end of **RESET** selects the parallel mode; held low at the end of **RESET** selects the serial mode. Each mode is described below.

Regardless of the interface mode chosen, the procedure to access the internal registers and memory of the ImageChip is the same. There is a 16-bit internal address register that is used as the address for the transfer. The address register must first be loaded by writing to its upper (ARH) and lower (ARL) bytes. A read or write cycle to the **ARH** accesses the internal upper 8-bit address register. A cycle to the **ARL** accesses the lower 8-bit address register. Reading or writing the data register (DR) then accesses the data. A cycle to the **DRI** accesses internal data addressed by the internal address register, with automatic post-increment of the address register.

Access to internal registers is accomplished by the particular mode selected by the **ADDRESS** lines, as shown in the following Table 4-1.

PROCESSOR ACCESS MODES	
Address [1:0]	**Target Transfer**
0 0	ARL; address register low bits [7:0]
0 1	ARH; address register high bits [15:8]
1 0	DR; data register
1 1	DRI; data register with address auto-increment

Table 4-1

Data writes are always 16-bits. Two 8-bit cycles are always required, and data is written to the target register or memory location during the second cycle. For example, to write to Control Register A (address 0x4000), the following sequence is used:

1. write 0x40 to **ARH**
2. write 0x00 to **ARL**
3. write lower 8 data bits to **DRI**
4. write upper 8 data bits to **DR**
   (or DRI if the next write is to the next sequential address)

Data reads can be either 8- or 16-bits. For example, to read to Control Register A (address 0x4000), the following sequence is used:

1. write 0x40 to **ARH**
2. write 0x00 to **ARL**
3. read lower 8 data bits from **DRI**
4. read upper 8 data bits from **DR**
(or DRI if the next read is to the next sequential address)

4.1.1 Parallel Processor Interface Mode

If the **$\overline{\text{WR}}$** pin is sampled high during **RESET**, the processor interface is 8-bit multiplexed asynchronous. The interface then consists of the following signals:

- **DATA – DATA**[7:0], pins 37 (MSB), 30-25, 22 (LSB)
- **ADDRESS – ADDRESS**[1:0], pins 39 (MSB), 38 (LSB)
- **CHIP SELECT – $\overline{\text{CS}}$**, pin 12
- **WRITE – $\overline{\text{WR}}$**, pin 41
- **READ – $\overline{\text{RD}}$**, pin 40

The parallel interface mode defaults to the little Endian mode. It can be put into the big Endian mode by setting Control Register B, Bit 5 to logic "1". Refer to Table 4-2 for byte ordering in both big and little Endian modes.

LITTLE ENDIAN BYTE ORDER	
15	0
byte 1	byte 0
byte 3	byte 2
byte 5	byte 4

BIG ENDIAN BYTE ORDER	
15	0
byte 0	byte 1
byte 2	byte 3
byte 4	byte 5

Table 4-2

4.1.2 Serial Processor Interface Mode

If the **$\overline{\text{WR}}$** pin is sampled low during RESET, the processor interface becomes bit serial. The interface then consists of the following signals:

- **SERIAL DATA – DATA**[0], pin 38
- **SERIAL CLOCK – DATA**[1], pin 25

The serial data is always made into a 13-bit “packet” as shown in Table 4-3.

SERIAL DATA PACKET					
Bit 0	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4..... Bit 11**	**Bit 12**
Address [0]	Address [1]	WR/	Hi-Z	Data [0].....Data [7]	Null

Table 4-3

The serial clock should be normally held high. Data is clocked on the falling edge of the serial clock. The header is 3 bits to indicate the type of transfer desired as shown in Table 4-1.

If Bit 2 is set, it is a read transfer, and the last 8-bits are read from the serial data pin There is a cycle of hi-Z before the read data. If Bit 2 is clear, it is a write cycle, and the last 8-bits are written to the specific target.

Bit 13 is a dummy bit used internally.

4.2 USING THE IMAGECHIP

Please note that information in this data sheet is provided for a 600 dpi print engine. Please contact Pixel Magic for information for use with print engines other than 600 dpi.

4.2.1 Initialization and Setup

The ImageChip provides a number of operating modes. Internal control registers and memory are used to setup and control the various modes. At power up, the control registers are initialized to their default state. The **LUT** memories and Line Store Memory come up in a random state. In order to activate any operating mode, specific values must be written to the control registers to set up the desired operating mode. The CPU must also download the engine characterization data to the **ILUT**, and the identity function data to the **PLUT**. The final data for the these tables is provided by Pixel Magic after a sampling of representative engines has been characterized. The internal Line Store Memory must be initialized from the CPU by loading all zeros into the memory.

The control registers and memory can be read by the host CPU to check status or hardware integrity. The address map for the control registers and internal memories are provided in the Control Register Functions section.

4.2.2 Power, Ground and PC Board Considerations

A multilayer board is preferred, with separate power, ground, and signal layers. If power and signals must be run on the same layer, then a ground plane must be used wherever possible. All **VDD** pins must be bypassed to the groundplane with 0.1µF capacitors, physically located as close to the pins as possible. The **LPVDD** connections must also be bypassed with 10µF and 0.01µF capacitors. An inductor should be used in place of the 0 Ohm resistor shown in Figure 4-3 if needed to improve performance, and to separate the **LPVDD** power bus.

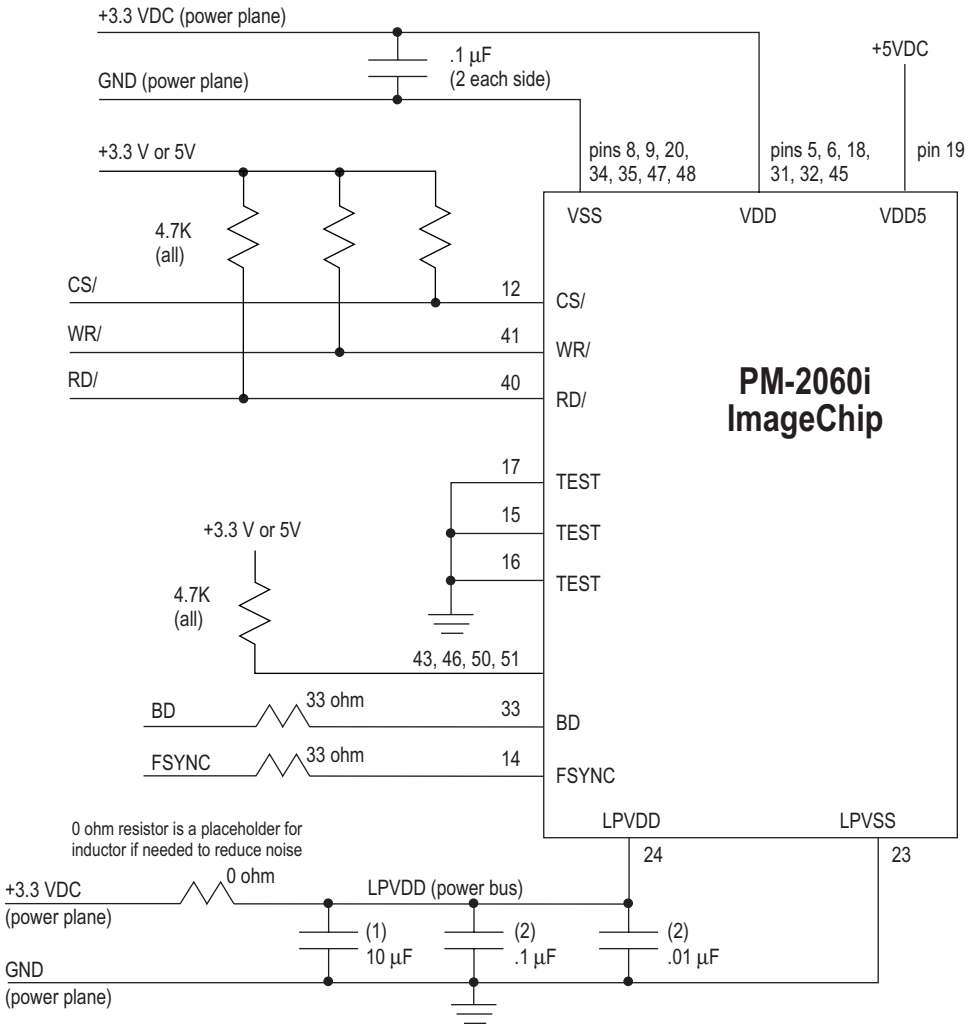
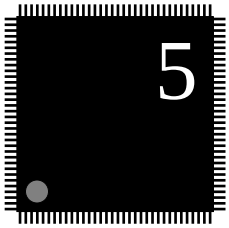


Figure 4-3

4.2.3 Input/Output Voltage Levels

The ImageChip is made up exclusively of low voltage (+3.3 V) chip interface circuits. However, all Input/Outputs (input-only, 3-state, or bi-directional) are 5 Volts tolerant, i.e. the corresponding pins can be connected to the buses which can swing between 0 V and 5 V. All unused inputs must be pulled to +3.3 V with a 4.7 kOhm resistor.



PM-2060i Register Descriptions

This chapter describes each of the PM-2060i's registers and all its fields, as well as the Contone Auto Positioning mode. These descriptions include information that is essential for programming the PM-2060i family of ImageChips.

Table of Contents

5.1 FUNCTIONAL BLOCKS

5.1.1 Control Register Functions

The internal control registers are all 16-bit wide. All accesses require two (2) 8-bit cycles to complete. The low byte (bits 7:0) is accessed with internal address bit [0] = 0. The high byte is accessed with internal address bit [0] = 1. Data is accessed low byte followed by high byte in little-Endian format. Please refer to the following table for the address map of the control registers and internal memories.

MEMORY MAP		
Address	**Location**	**Region**
0 x 0 0 0 0 0 x 0 3 f f	Calibration Memory (ILUT) 512 x 10	Memory
0 x 1 0 0 0 0 x 11 f f	Postion Memory (PLUT) 256 x 8	
0 x 2 0 0 0 0 x 3 f f f	Line Store Memory 4096 x 16	
0 x 4 0 0 0	Control Register A	Control
0 x 4 0 0 2	Control Register B	
0 x 4 0 0 4	Control Register C	
0 x 4 0 0 6	Control Register D	
0 x 4 0 0 8	Control Register E	
0 x 4 0 0 a	Control Register F	
0 x 4 0 0 c	Prime Register	
0 x 4 0 0 e	Left Margin Register	
0 x 4 0 1 0	Line Length Register	
0 x 4 0 1 2	Top Margin Register	
0 x 4 0 1 4	Lines Register	
0 x 4 0 1 a	Revision Register	
0 x 4 0 2 0 0 x 7 f f f	Reserved	
0 x 8 0 0 0 0 x 8 f f f	Reserved	Modulator

Table 5-4

5.1.2 Control Register A

Address: 0x4000; read/write; Reset to 0x0700

Control Register A provides most of the mode and operating control bits for the ImageChip.

CONTROL REGISTER A						
Bits	**Name**					**Function**
0	Software Reset					0 = Normal operation 1 = Reset state
4:1	Mode	**D4**	**D3**	**D2**	**D1**	**Mode**
		0	0	0	0	600 x 1 Enh. Text Only
		0	0	0	1	600 x 1 Test (EEU Bypassed)
		0	0	1	0	Not used
		0	0	1	1	Not used
		0	1	0	0	300 x 1 Enhanced Text
		0	1	0	1	300 x 1 Test (EEU Bypassed)
		0	1	1	0	200 x 1 Enhanced Text
		0	1	1	1	200 x 1 Test (EEU Bypassed)
		1	0	0	0	200 x 100 x 1 Enhanced Text
		1	0	0	1	200 x 100 x 1 Test (EEU Bypassed)
		1	0	1	0	1200 x 1 Enhanced Text
		1	0	1	1	600 x 8 Multi-Bit*
		1	1	0	0	300 x 8 Multi-Bit*
		1	1	0	1	600 x 1B 6-Bit Gray, 2-Bit Position*
		1	1	1	0	Not used
		1	1	1	1	600 x 4 Multi-Bit*
7:5	Pixel Magic Reserved					Set to logic “111” for normal operation
9:8	LUT Bypass	**D8**	**D9**			**LUT Bypass**
		0	0			No Bypass
		0	1			PLUT Bypassed
		1	0			ILUT Bypassed
		1	1			ILUT & PLUT Bypassed
10	Frame Sync Enable					0 = Disabled 1 = Enabled
12:11	Video Source Select	**D12**	**D11**			**Video Source**
		0	0			Parallel
		0	1			not used
		1	0			not used
		1	1			Serial
13	150 Line Screen Select					0 = Disables 150 line screen output 1 = Enables 150 line screen output
14	CPU To Internal LUT					0 = Normal operation 1 = CPU Access to LUTs
15	CPU To Line Store					0 = Normal operation 1 = CPU access to Line Store

*PM-2060i and PM-2040i only

Table 5-5

Bits 0 **Software Reset**

Resets the ImageChip. It is OR'd with the **$\overline{\text{RESET}}$** pin (21). Normal operation is with the bit set to "0"; a reset state occurs with the bit set to "1".

Bits 4:1 **Mode**

Bits 4:1 control the enhancement mode of the ImageChip. Each of the enhancement modes is discussed in detail elsewhere in this document.

Bits 7:5 **Pixel Magic Reserved**

These bits are reserved by Pixel Magic. They must be set to a logic "111" for normal operations.

Bits 9:8 **LUT Bypass**

Bits 9:8 determine which internal LUTs are bypassed. Reset condition is both bits are set to logic "1", which bypasses both LUTs.

Bit 10 **FSync Enable**

Bit 10 set to logic "1" enables the **FSYNC** (frame sync) signal; bit 10 set to logic "0" disables the **FSYNC** signal. FSync Enable synchronizes the top of page (synch) to the line syncs. With bit 10 at logic 0, the **BEAM DETECT** signal is ignored. Bit 10 is set by the software to begin a page. With bit 10 high, **FSYNC** enables the counting of **LSYNC** clocks, which, prior to the start of data transfer to the print engine, represents the vertical margin. It is not required to be cleared and set in between multi-page documents or color planes. The start of a page, beyond the first page in a job, is automatically synchronized to the **FSYNC** signal. When the print job is completely finished, bit 10 should be cleared and then set again in order to ensure page synchronization for the next print job.

Bits 12:11 **Video Source Select**

Bits 12:11 select from two sources for input video data. Parallel video data can be input from the **PARALLEL VIDEO INPUT** pins (52, 1, 2, 3, 4, 7, 10, 11). Serial video data is input from the **SERIAL VIDEO INPUT** pin (11). Video data is input in conjunction with the **SOURCE VIDEO CLOCK OUTPUT** pin (44).

Bit 13 **150 Line Screen Select**

Bit 13 controls the selection of optional 150 line screen processing of grayscale images. Setting this bit to a logic "1" selects a 150 horizontal line screen in either the 600 x 8 or 300 x 8 output modes. This coarser screen reduces the effect of engine noise (banding) on the output image.

Bit 14 CPU To Internal LUT

Bit 14 is the **READ/WRITE** control line for the internal **LUT** memories **ILUT** and **PLUT**. When set to a logic "1", the bi-directional path into the **LUT** memories is enabled. This allows the **LUT** memories to be written and read from the external address and data lines. When set to a logic "1", it allows calibration table data to be downloaded to the **ILUT**, and pulse position modification table data to be downloaded to the **PLUT**. Set this bit to "0" for normal printing operations. (Refer to "LUT Memories" on page 5-16.)

Bit 15 CPU To Internal Line Store

Bit 15 is the **READ/WRITE** control line for the internal Line Store Memory. When this bit is set to a logic "1", the bi-directional path into the Line Store Memory is enabled. Set this bit to "0" for normal printing operations. (Refer to "Line Store Memory" on page 5-18.)

5.1.3 Control Register B

Address: 0x4002; read/write; Reset to 0x0000

Control Register B provides bits to control various internal operating parameters of the ImageChip.

CONTROL REGISTER B					
Bits	**Name**	**Function**			
1-0	Clock Divider Ratio	**D1**	**D0**	**Divider Ratio:**	
		0	0	1	
		0	1	2	
		1	0	4	
		1	1	8	
2	Reserved	Set = "0"			
3	Parallel Video Source Endian Control	0 = Normal; big endian 1 = Little endian			
4	Serial Video Shift Direction	0 = Shift left 1 = Shift right			
5	Big Endian CPU Interface	0 = Little endian 1 = Big endian			
6	Clear Line Store Memory	0 = Normal operation 1 = Clear Line Store Memory			
7	Continuous Print	0 = Normal page length 1 = Infinite page length			
10:8	Serial Byte Align	**D10**	**D9**	**D8**	**Alignment**
		0	0	0	7:0
		0	0	1	8:1
		0	1	0	9:2
		0	1	1	10:3
		1	0	0	11:4
		1	0	1	12:5
		1	1	0	13:6
		1	1	1	14:7
12:11	Not Used	Set = "0"			
13	Test Data Enable	Set = "0"			
15:14	Not Used	Set = "0"			

Table 5-6

Bits 1:0 Clock Divider Mode

Bits 1:0 determine the divisor for the external clock oscillator applied to the **PRINTER VIDEO CLOCK INPUT** pin (49).

Bit 2 Reserved

This control register bit is reserved, always set to "0".

Bit 3 Parallel Video Source Endian Control

Controls the byte order of the parallel source video data. The default for Bit 3 is a logic “0”, which is normal big Endian mode. Setting Bit 3 to a logic “1” implements little Endian mode.

Bit 4 Serial Video Shift Direction

Bit 4 controls the shift direction of the serial video data when input through the serial interface. Bit 4 determines whether the high order bit (Bit 7) or the low order bit (Bit 0) of any given 8-bit video data word is to be considered the left-most bit, and therefore output first to the print engine. With Bit 4 set to a logic “0”, the most significant bit is first; with Bit 4 set to a logic “1”, the least significant bit is first.

Bit 5 Big Endian CPU Interface

Bit 5 controls the byte order of data at the CPU data bus. With Bit 5 set to a logic “0”, the big Endian mode is selected; with Bit 5 set to a logic “1”, the little Endian mode is selected. Refer to the figure below.

LITTLE ENDIAN BYTE ORDER	
15	0
byte 1	byte 0
byte 3	byte 2
byte 5	byte 4

BIG ENDIAN BYTE ORDER	
15	0
byte 0	byte 1
byte 2	byte 3
byte 4	byte 5

Table 5-7

Bit 6 Clear Line Store Memory

When Bit 6 is set to a logic “1”, the Line Store Memory is cleared at the end of the active vertical page, as determined by the count in the vertical bottom margin register. If the vertical data is being padded with null lines to flush the data in the Line Store Memory, then the action controlled by this bit is redundant. If the vertical data is not being padded with null lines, then this bit must be set in order to avoid leaving any data in the Line Store memories to be imaged at the beginning of the succeeding page. Bit 6 should be set to a logic “0” for normal operation.

Bit 7 Continuous Print

When Bit 7 is set to a logic “1”, the continuous print mode is enabled. When active, continuous print mode allows an infinite number of lines to be printed. Bit 7 should be set to a logic “0” for normal operation.

Bits 10:8 Serial Byte Alignment

Bits 10:8 provide an adjustment for aligning the start of eight bit data when transferred through the serial interface to the ImageChip. After an LSync goes low, it is assumed that Bit 7 of the video data is valid at the rising edge of the very first source clock pulse. When the system providing the data needs several clock cycles to get the data to the ImageChip, bits 10-8 provide for this delay. A selection of 000 corresponds to a delay of 0 clock periods; a selection of 111 corresponds to a delay of seven (7) clock periods.

Bits 12:11 Not Used

These control register bits are not used, always set to “0”.

Bit 13 Test Data Enable

Reserved for Pixel Magic. Bit 13 must be set to a logic “0” for proper ImageChip operation.

Bits 15:14 Not Used

These control register bits are not used, always set to “0”.

5.1.4 Control Register C

Address: 0x4004; read/write; Reset to 0xa1e0

Control Register C provides control over input and output signal polarities.

CONTROL REGISTER C				
Bits	**Name**	**Function**		
4:0	Not Used	Set = “0”		
5	Beam Detect Input Polarity	0 = Rising edge 1 = Falling edge		
6	Frame Sync Input Polarity	0 = Rising edge 1 = Falling edge		
7	EOP Output Polarity	0 = Active high 1 = Active low		
8	Line Sync Output Polarity	0 = Active high 1 = Active low		
9	Source Video Clock Output Polarity	0 = Clock on rising edge 1 = Clock on falling edge		
10	Modulator Reset	0 = Normal operation 1 = Modulator reset		
11	Video Input Polarity	0 = Normal video; “0” is white 1 = Reverse video; “1” is white		
12	Video Output Polarity	0 = Normal video; “0” is white 1 = Reverse video; “1” is white		
13	Video Output Enable	0 = Video enabled 1 = Video disabled		
15:14	Video Mode	**D15**	**D14**	**Video Mode**
		0	0	Normal
		0	1	Reverse normal
		1	0	Force white (black pulses)
		1	1	Force black (white pulses)

Table 5-8

Bits 4:0 Not Used

These control register bits are not used, always set to “0”.

Bit 5 Beam Detect Input Polarity

When Bit 5 is set to a logic “0”, the rising edge of the **BEAM DETECT** signal is used; when Bit 5 is set to a logic “1”, the falling edge of the **BEAM DETECT** signal is used. Bit 5 is reset to a logic “1”, falling edge.

Bit 6 Frame Sync Input Polarity

When Bit 6 is set to a logic “0”, the rising edge of the **FSYNC** signal is used; when Bit 6 is set to a logic “1”, the falling edge of the **BEAM DETECT** signal is used. Bit 6 is reset to a logic “1”, falling edge.

Bit 7 End of Page Output Polarity

When Bit 7 is set to a logic “0”, the **EOP** signal is active high; when Bit 7 is set to a logic “1”, the **EOP** signal is active low. Bit 7 is reset to a logic “1”, active low.

Bit 8 Line Sync Output Polarity

When Bit 8 is set to a logic “0”, the **LSYNC** signal is active high; when Bit 8 is set to a logic “1”, the **LSYNC** signal is active low. Bit 8 is reset to a logic “1”, active low.

Bit 9 Source Video Clock Output Polarity

When Bit 9 is set to a logic “0”, data is clocked on the rising edge of the **SOURCE VIDEO CLOCK OUTPUT**; when Bit 9 is set to a logic “1”, data is clocked on the falling edge of the **SOURCE VIDEO CLOCK OUTPUT**. Bit 9 is reset to a logic “1”, falling edge.

Bit 10 Modulator Reset

When Bit 10 is set to a logic “1”, the modulator is reset. Bit 10 should be set to a logic “0” for normal operation.

Bit 11 Video Input Polarity

When Bit 11 is set to a logic “0”, input video is normal, i.e. “0” is white; when Bit 11 is set to a logic “1”, input video is reversed, i.e. “1” is white.

Bit 12 Video Output Polarity

When Bit 12 is set to a logic “0”, output video is normal, i.e. “0” is white; when Bit 12 is set to a logic “1”, output video is reversed, i.e. “1” is white.

Bit 13 Video Output Enable

When Bit 13 is set to a logic “1”, the video output is disabled. Bit 13 should be set to a logic “0” for normal operation. Bit 13 is reset to a logic “0”, video output enabled.

Bit 15:14 Video Mode

Bits 15:14 control the video mode. Reset to 10, force white (black pixels).

5.1.5 Control Register D

Address: 0x4006; read/write; Reset to 0x0000

Control Register D provides control over printing data.

CONTROL REGISTER D		
Bits	**Name**	**Function**
2:0	Parallel Source Video Pipeline Prime Pulses	000 = Disables priming 111 = Not allowed
8:3	Reserved	Set = “0”
13:9	LSync Width	Width of LSync output pulse in pixel clocks
14	Contone Auto Position Enable*	0 = Multibit edge enhancement disabled 1 = Multibit edge enhancement enabled
15	Contone Auto Position Reverse*	0 = Normal video 1 = Reverse video

* PM-2060i and PM-2040i only

Table 5-9

Bits 2:0 Parallel Source Video Pipeline Prime Pulses

Bits 2:0 contains the number of source video clock prime pulses. A value of 000 disables priming. A value of 111 is not allowed.

Bits 8:3 Reserved

These bits are reserved for Pixel Magic, always set to “0”.

Bits 13:9 LSync Width

Bits 13:9 control the width of the **LSYNC** output signal, in pixel clocks.

Bit 14 Contone Auto Position Enable

This bit is valid in 4- and 8-bit modes only. When Bit 14 is set to a logic “0”, the contone auto position processing is disabled; when Bit 14 is set to a logic “1”, the contone auto position processing is enabled. Refer to “Contone Auto Positioning Mode (PM-2060i and PM-2040i only)” on page 5-18. Set to “0” for PM-2020i and PM-2010i.

Bit 15 Contone Auto Position Reverse

This bit is valid in 4- and 8-bit modes only. When Bit 15 is set to a logic “0”, the contone auto position processing outputs normal video; when Bit 15 is set to a logic “1”, the contone auto position processing outputs reversed video. Set to “0” for PM-2020i and PM-2010i.

5.1.6 Control Register E (PM2060i and PM2040i only)

Address: 0x4008; read/write; Reset to 0xff00

Control Register E provides control for edge detection thresholds for the contone auto positioning modes. Refer to “Contone Auto Positioning Mode (PM-2060i and PM-2040i only)” on page 5-18.

CONTROL REGISTER E		
Bits	**Name**	**Function**
7:0	Multi-Bit Bottom	Lower edge detection threshold
15:8	Multi-Bit Top	Upper edge detection threshold

Table 5-10

Bits 7:0 Multi-Bit Bottom [7:0]

These register bits control the lower edge detection threshold value. They are normally set to 0x00.

Bits 15:8 Multi-Bit Top [7:0]

These register bits control the upper edge detection threshold value. They are normally set to 0xff.

5.1.7 Control Register F

Address: 0x400a; read/write; Reset to 0x0000

Control Register F provides control over the line phase shift of the video modulator.

CONTROL REGISTER F		
Bits	**Name**	**Function**
7:0	Line Phase	0 x 0 0 = No shift 0 x f f = shift by whole cell position
15:8	Reserved	Set = “0”

Table 5-11

Bits 7:0 Line Phase

Bits 7:0 provide an offset to the start of each pixel cell. This is typically used at the start of a color plane to provide registration between colors in a multi-pass system. When used this way, the entire image is shifted by a fraction of a cell controlled by the line phase value. 0x00 is no shift, and 0xff is shift by a whole cell position relative to the Beam Detect input.

Bits 15:8 Reserved

These bits are reserved for Pixel Magic, always set to 0.

5.1.8 PRIME Register

Address: 0x400c; write-only; Reset to n/a

PRIME REGISTER		
Bits	**Name**	**Function**
15:0	Prime Data	Command used to prime source video pipeline

Table 5-12

The **PRIME** register is a write-only register used to enable the source video pipeline priming at the start of a page or group of multi-color pages. It should be written to:

- after the Parallel Source Video Pipeline Prime Pulses — Bits 2:0 — value has been written to Control Register D.
- before the start of the page
- when the source video data pipeline is empty

This register is not used when no priming is required. Control Register D, Bits 2:0 are then set = 0.

5.1.9 LEFT MARGIN Register

Address: 0x400e; read/write; Reset to 0x0000

LEFT MARGIN REGISTER		
Bits	**Name**	**Function**
15:0	Left Margin	Number of output cell clocks from active edge of Beam Detect to left edge of image Parallel Video: Register = Left Margin - 22 Serial Video: Register = 0 x 0000

Table 5-13

This register is used to specify the left margin. It counts the number of output cell clocks starting from the active edge of **BEAM DETECT** to when the left edge of the image begins. It should be loaded as follows:

MODE	**LEFT MARGIN REGISTER VALUE**
Parallel Video	Left Margin – 22
Serial Video	0x0000

5.1.10 LINE LENGTH Register

Address: 0x4010; read/write; Reset to 0x0000

LINE LENGTH REGISTER						
Bits	**Name**	**Function**				
15:0	Line Length	Number of printed pixels resulting from a given number of source bytes per line				
		Mode (Control Reg. A; Bits 4:1)				**Line Length Register Value***
		D4	**D3**	**D2**	**D1**	
		0	0	0	0	SRCBYTES* 8 - 1
		0	0	0	1	SRCBYTES* 8 - 1
		0	0	1	0	SRCBYTES* 8 - 1
		0	0	1	1	SRCBYTES* 8 - 1
		0	1	0	0	2*SRCBYTES* 8 - 1
		0	1	0	1	2*SRCBYTES* 8 - 1
		0	1	1	0	3*SRCBYTES* 8 - 1
		0	1	1	1	3*SRCBYTES* 8 - 1
		1	0	0	0	3*SRCBYTES* 8 - 1
		1	0	0	1	3*SRCBYTES* 8 - 1
		1	0	1	0	SRCBYTES* 8/2/2 - 1
		1	0	1	1	SRCBYTES - 1
		1	1	0	0	2*SRCBYTES - 1
		1	1	0	1	2*SRCBYTES - 1
		1	1	1	0	SRCBYTES* 8 - 1
		1	1	1	1	SRCBYTES* 8/4 - 1
		Serial Video All Modes				0 x f f f f

* SRCBYTES = number of source bytes contained in each line.
SRCBYTES must be an even number

Table 5-14

The **LINE LENGTH** register is used to specify the line length. It should always be set to a non-zero value. It specifies the number of printed pixels resulting from a given number of source bytes per line. It should be loaded as shown. **SRCBYTES** is the number of source bytes contained in each line. **SRCBYTES** must be an even number.

5.1.11 TOP MARGIN Register

Address: 0x4012; read/write; Reset to 0x0000

TOP MARGIN REGISTER			
Bits	**Name**	**Function**	
15:0	Top Margin	Number of Beam Detect pulses, starting with the first BD after FSync at the beginning of a page.	
		Source Video	**Value**
		Parallel	Top Margin + 1
		Serial	0 x 0 0 0 0

Table 5-15

This register is used to specify the top margin. It counts **BEAM DETECT** (start of lines) starting with the first **BEAM DETECT** after the **FSYNC** signal at the beginning of the page. It should be loaded as follows:

MODE	**TOP MARGIN REGISTER VALUE**
Parallel Video	Top Margin +1
Serial Video	0x0000

5.1.12 LINES Register

Address: 0x4014; read/write; Reset to 0x0000

LINES REGISTER						
Bits	**Name**	**Function**				
15:0	Printed Lines	Number of printed lines in each page				
		Mode (Control Reg. A; Bits 4:1)				**Lines Register Value***
		D4	**D3**	**D2**	**D1**	
		0	0	0	0	SRCLINES
		0	0	0	1	SRCLINES
		0	0	1	0	SRCLINES
		0	0	1	1	SRCLINES
		0	1	0	0	2*SRCLINES
		0	1	0	1	2*SRCLINES
		0	1	1	0	3*SRCLINES
		0	1	1	1	3*SRCLINES
		1	0	0	0	6*SRCLINES
		1	0	0	1	6*SRCLINES
		1	0	1	0	SRCLINES
		1	0	1	1	SRCLINES
		1	1	0	0	2*SRCLINES
		1	1	0	1	SRCLINES
		1	1	1	0	SRCLINES
		1	1	1	1	SRCLINES
		Serial Video All Modes				0 X f f f f

* SRCLINES = number of lines contained in the source image data.

Table 5-16

This register is used to specify the number of printed lines in each page. It should be loaded as shown. **SRCLINES** is the number of lines contained in the source image data.

5.1.13 LUT Memories

The 2060i has two Look Up Table (LUT) memories used to modify the video data prior to its output to the printer engine calibration (**ILUT**) memory and position (**PLUT**) memory.

5.1.13.1 Calibration (ILUT) Memory

The first **LUT**, the calibration or **ILUT**, stores a set of characterization data for the printer engine that translates the fixed image values generated by the page description language to values that will reproduce the highest quality image possible. These new values take into account all of the variables that affect print quality including engine linearity, temperature, aging, environment, and toner exhaustion, as well as printer features such as the amount of toner, paper type, and type of input. Each of these variables must be compensated for in order to maintain high quality image output.

The characterization data that is loaded in to the **LUT** by the host CPU is provided by Pixel Magic. It is derived from extensive testing on a variety of print engines, and a representative sampling of the actual engine which will be used in your particular product.

The **ILUT** is organized as two 256x10 memories, but is referred to as a single **LUT** memory. In single-bit modes (modes 0 through 10, and 14) only **LUT** 0 is used. In multi-bit modes (modes 11 through 13, and 15) both **LUTS** are used, one for odd scan lines, and the other for even scan lines (standard mode). In the standard mode, they are used in the sequence 0, 1, 0, 1, 0, 1, …. In the 150 line screen select mode (Control Register A, Bit 13), they are used in the sequence 0, 1, 1, 0, 0, 1, 1, 0, 0, …; this produces a 150 horizontal line screen.

To **LOAD** or **READ** the **ILUT** memory, Bit 14 in Control Register A is asserted. Subsequent reading or writing to memory locations 0x0000-0x03ff will address the **ILUT** memory.

It is important that the CPU to Internal **LUT** bit (Control Register A, Bit 14) is cleared before attempting to print.

5.1.13.2 Position (PLUT) Memory

The second **LUT** memory within the 2060i is the position **LUT**, or **PLUT**. In special circumstances, data loaded into the 256x8 **PLUT** would be used to modify video pixel position data prior to being fed to the modulator for output to the printer engine. Under normal operating conditions however, the PLUT is loaded with an identity function, i.e., no position modification is performed. The identity function data is provided by Pixel Magic.

To **LOAD** or **READ** the **PLUT** memory, Bit 14 in Control Register A is asserted. Subsequent reading or writing to memory locations 0x1000-0x11ff will address the **PLUT** memory.

It is important that the CPU to Internal **LUT** bit (Control Register A, Bit 14) is cleared before attempting to print.

5.1.14 Line Store Memory

The Line Store Memory (LSM) is a 16-bit buffer used to hold the source video data. It is large enough to hold 8 lines of 600 dpi 1-bit data. Multiple lines of data are stored and accessed from the memory as a 9x10 “window” of data that is used by the Edge Enhancement Units. The Line Store Memory/Control Logic captures the parallel or serial video source data. Parallel source data is demultiplexed into 16 bits before being written to the memory. There is Endian control for parallel source video modes (Control Register B, Bit 3), allowing the byte data loading to be reversed. The Line Store Memory is not used for the 600x8 operating modes.

To **LOAD** or **READ** the **LSM**, Bit 15 in Control Register A is asserted. Subsequent reading or writing to memory locations 0x2000-0x3fff will address the **LSM**.

It is important that the CPU to Line Store bit (Control Rgister A, Bit 15) is cleared before attempting to print. This memory must be entirely cleared before printing the first page after power-up.

5.1.15 Contone Auto Positioning Mode (PM-2060i and PM-2040i only)

The 2060i and 2040i provide a contone auto position feature for the 600x8 and 600x4 operating modes. In this mode, the multi-bit data represents the shade of gray on paper. This is achieved by varying the width of the pulse within a given cell. Given that the pulses are normally centered within each cell, along the edge of a solid feature, this could be printed as a fragmented edge, i.e. "random" dots separated by white space. The contone auto position mode detects the solid white to solid black transistions, and for the shades of gray in between, force justifies the position of the varying width pulses, either left or right, against the solid black cell.

The contone auto positioning mode is controlled by the following:

- Control Register D, Bit 14 enables and disables the processing
- Control Register D, Bit 15 selects a normal or reverse edge
- Control Register E, Bits 15:8 provide the top edge detection threshold
- Control Register E, Bits 7:0 provide the bottom edge detection threshold

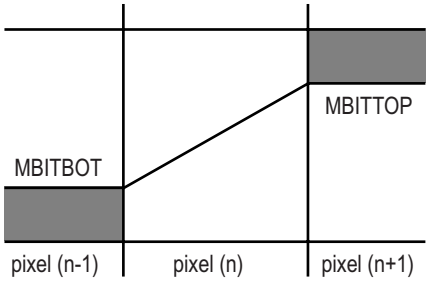


Figure 5-4

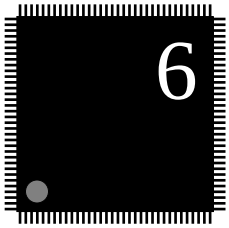
5.2 OPERATING MODE SUMMARY

A table summarizing all control register bits set for normal operation is shown below.

CONTROL REGISTER BIT SUMMARY				
Control Register	**Bits**	**Function**		**Value***
A	4:1	Operating Mode		0 - F
	10	Frame Sync Enable		1
	12:11	Video Source Select - Parallel		00
		Video Source Select - Serial		11
	13	150 Line Screen		0 or 1
	14	CPU to Internal LUT		0
	15	CPU to Line Store		0
B	6	Clear Line Store Memory		0
	13	Test Data Enable		0
C	5	Beam Detect Input Polarity		0 or 1
	6	Frame Sync Input Polarity		0 or 1
	7	EOP Input Polarity		0 or 1
	8	Line Sync Output Polarity		0 or 1
	9	Source Video Clock Output Polarity		0 or 1
	10	Modulator Reset		0
	11	Video Input Polarity		0 or 1
	12	Video Output Polarity		0 or 1
	13	Video Output Enable		0 or 1
	15:14	Video Mode		00 or 11
D	2:0	Parallel Source Video Pipeline Prime Pulses		0h - 6h
	13:9	L Sync Width		0h - 1Fh
	14	Contone Auto Position		0 or 1
	15	Contone Auto Position Reverse		0 or 1
E	7:0	Lower Edge Detection Threshold		0 x 0 0
	15:8	Upper Edge Detection Threshold		0 x f f
F	7:0	Line Phase Shift		0 x 0 0 – 0 x f f
PRIME	15:0	Prime Data		
LEFT MARGIN	15:0	Left Margin	Parallel Video	Left Margin – 22
			Serial Video	0 x 0 0 0 0
LINE LENGTH	15:0	Line Length	Parallel Video	Line Length
			Serial Video	0 x f f f f
TOP MARGIN	15:0	Top Margin	Parallel Video	Top Margin + 1
			Serial Video	0 x 0 0 0 0
LINES	15:0	Printed Lines/Page	Parallel Video	0 0 0 0 – f f f f
			Serial Video	0 x f f f f

*Underscore value denotes enabled or normal state.

Table 5-17



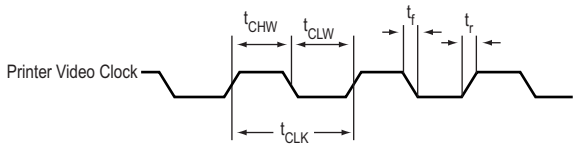
PM-2060i Timing Diagrams

This chapter presents the AC timing diagrams for all data transactions on the PM-2060i.

Table of Contents

6.1 Timing Diagrams and AC Characteristics

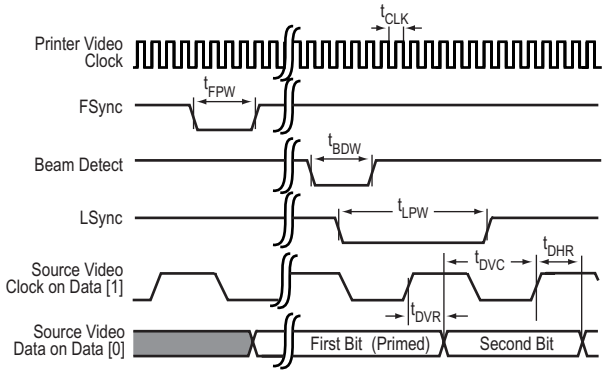
Printer Video Clock Timing



Parameter	Symbol	Min.	Max.	Unit
Clock period	t_{CLK}	15.0	333	ns
Clock high pulse width	t_{CHW}	0.4 x t_{CLK}	0.6 x t_{CLK}	ns
Clock low pulse width	t_{CLW}	0.4 x t_{CLK}	0.6 x t_{CLK}	ns
Clock rise time	t_r	—	2.0	ns
Clock fall time	t_f	—	2.0	ns

Table 6-18

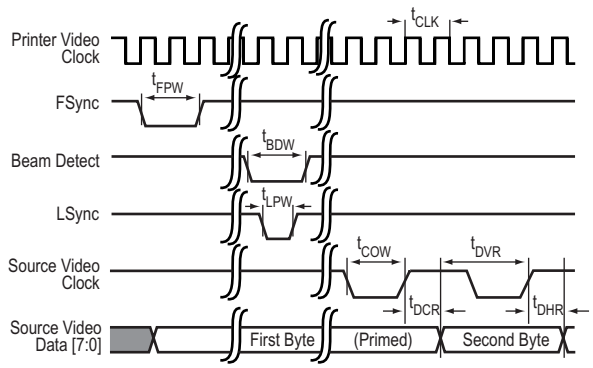
Serial Video Timing



Parameter	Symbol	Min.	Max.	Unit
FSync input pulse width	t_{FPW}	2 x t_{CLK}	—	ns
Beam Detect input pulse width	t_{BDW}	2 x t_{CLK}	—	ns
LSync output pulse width	t_{LPW}	1 x t_{CLK}	32 x t_{CLK}	ns
Source video data valid from source video clock rising edge	t_{DVR}	—	t_{CLK} - t_{DVC}	ns
Source video data valid to source video clock rising	t_{DVC}	7.0	—	ns
Source video data hold from rising source video clock	t_{DHR}	0.0	—	ns

Table 6-19

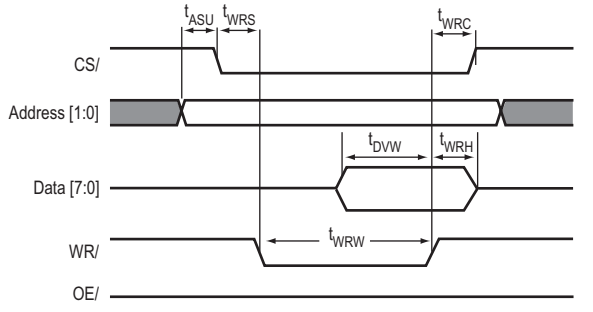
Parallel Video Timing



Parameter	Symbol	Min.	Max.	Unit
FSync input pulse width	t_{FPW}	2 x t_{CLK}	—	ns
Beam Detect input pulse width	t_{BDW}	2 x t_{CLK}	—	ns
LSync output pulse width	t_{LPW}	1 x t_{CLK}	32 x t_{CLK}	ns
Source video clock output pulse width	t_{COW}	0.5 x t_{CLK}	—	ns
Source video data valid to source video clock rising	t_{DVR}	7.5	—	ns
Source video data changes with source video clock rising edge	t_{DCR}	—	t_{CLK} - t_{DVR}	ns
Source video data hold from rising source video clock	t_{DHR}	0.0	—	ns

Table 6-20

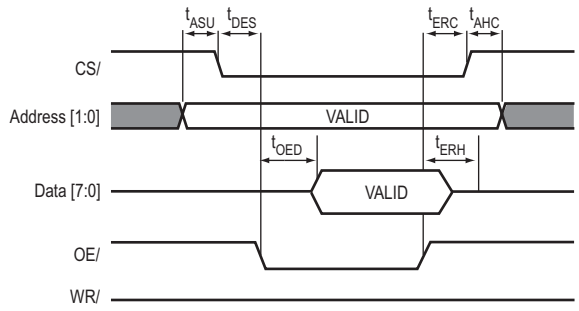
CPU Interface Write Timing



Parameter	Symbol	Min.	Max.	Unit
Address Valid to CS/ falling	t_{ASU}	0.0	—	ns
CS/ falling to WR/ falling	t_{WRS}	0.0	—	ns
Data valid to WR/ rising (end of cycle)	t_{DVW}	4.5	—	ns
WR/ rising to CS/ rising	t_{WRC}	8.5	—	ns
WR/ rising to Data hold	t_{WRH}	4.0	—	ns
WR/ low pulse width	t_{WRW}	10.0	—	ns

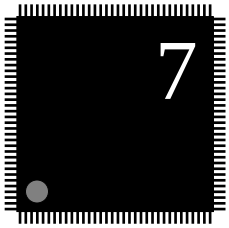
Table 6-21

CPU Interface Read Timing



Parameter	Symbol	Min.	Max.	Unit
Address Valid to CS/ falling	t_{ASU}	0.0	—	ns
CS/ falling to OE/ falling	t_{DES}	0.0	—	ns
OE/ falling to Data valid	t_{OED}	—	5.0	ns
OE/ rising to Data hold	t_{ERH}	2.5	—	ns
OE/ rising to CS/ rising	t_{ERC}	0.0	—	ns
Address hold from CS/ rising	t_{AHC}	0.0	—	ns

Table 6-22



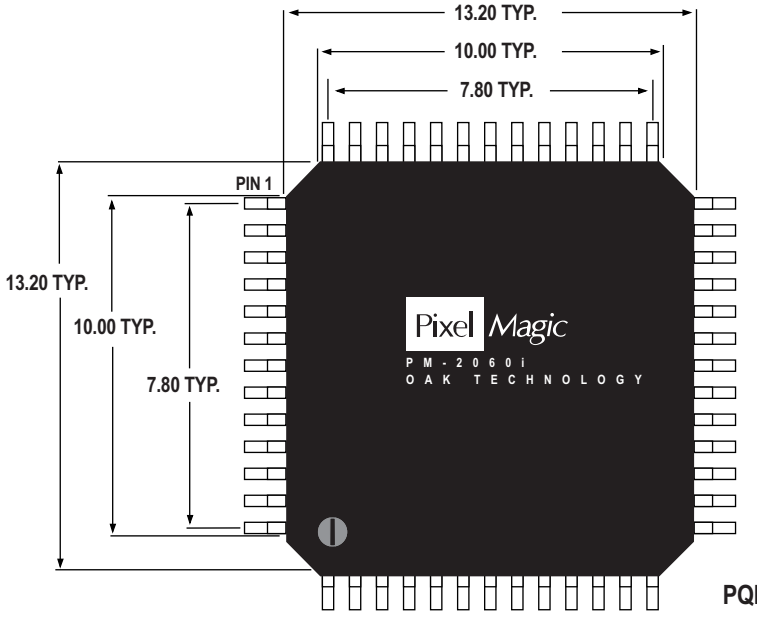
PM-2060i Package Information

This chapter provides information about the PM-2060i package, including its dimensions, pin characteristics, and pin locations.

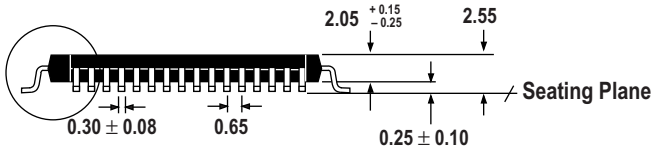
Table of Contents

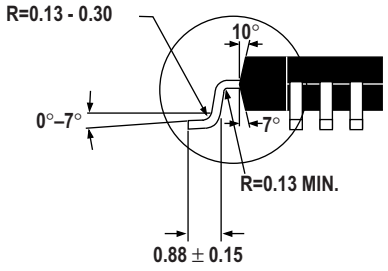
7.1 Package Dimensions

The PM-2060i is fabricated using a CMOS process and is packaged in an industry-standard metric 52-pin Plastic Quad Flat Pack (PQFP).



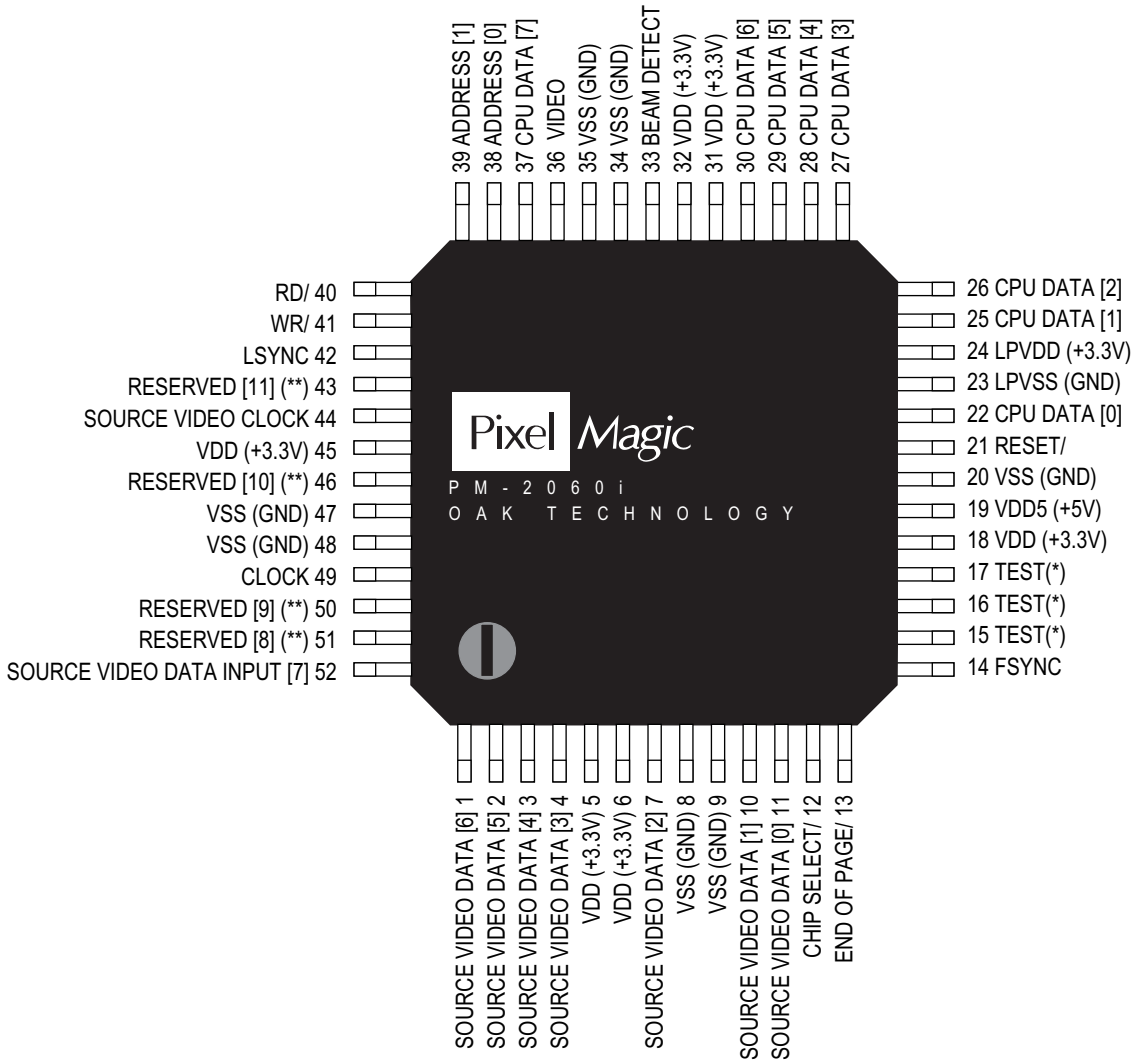
PQFP PACKAGE





All dimensions are in millimeters

7.2 Pin Arrangement



(*) Reserved for Pixel Magic; tie to VSS (GND); make no other connection

(**) Reserved for Pixel Magic; tie to VDD (+3.3 V) through 4.7 kOhm resistor; make no other connection

Pixel Magic, Inc.
300 Brickstone Square
Andover, MA 01810
VOICE: +1-978-470-8830
FAX: +1-978-470-8892
WEB: www.pixelmagic.com

•

Pixel Magic, Inc. – Japan
Oak Technology, K.K.
Musashino Nissay Plaza 5F
1-11-4 Nakamachi
Musashino City
Tokyo, Japan 180
VOICE: +81-422-56-3761
FAX: +81-422-56-3778

•

Pixel Magic, Inc. – Taiwan
Oak Technology, Inc.
Room B, 7F, No. 370
Section 1, Fu Hsing South Road
Taipei, Taiwan R.O.C.
VOICE: +886-2-784-9123
FAX: +886-2-706-7641